

# M52039SP

## PAL/NTSC VIDEO CHROMA DEFLECTION

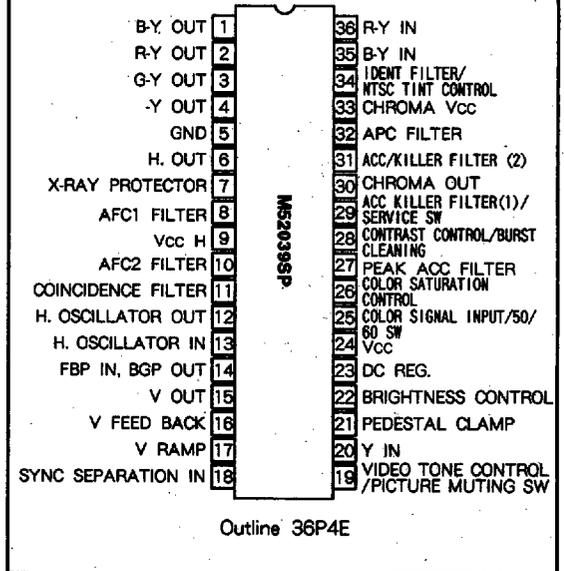
### DESCRIPTION

The M52039SP is a semiconductor integrated circuit for video, chroma, and deflection signal processing. Combined with integrated component M51346AP for VIF/SIF, it realizes practical color television using only two IC components. Circuit configuration includes built-in sync separation, horizontal AFC, horizontal oscillator, horizontal count-down, vertical count-down, contrast control, luminance control, video tone control, ACC/killer detector, ident detector, APC detector, chroma oscillator, NTSC tint control, and chroma demodulator functions.

### FEATURES

- PAL/NTSC/SECAM multi-system processing can be realized by adding IC component M52026SP for processing SECAM chroma signals.
- Large-scale, single-chip construction enhances practicality and reliability of the television set itself while contributing to lower power consumption.
- Places of adjustment and number of external components are minimized.
- NTSC system switch enables construction of a PAL/NTSC system with a minimal amount of peripheral components. (Switches demodulator axis, demodulation ratio, PAL matrix, and tint control.)
- Double AFC in the horizontal circuit effectively reduces weak electric field horizontal "jitter," and minimizes "bending" on the screen caused by luminance alteration. Coincidence detector circuit not only expands horizontal pull-in range, but can be used as a sensor signal for sound muting, automatic channel selection, etc.
- Contains built-in service switch. (Contrast minimum killer on, vertical output off)

### PIN CONFIGURATION (TOP VIEW)



### APPLICATION

PAL/SECAM Dual, PAL/SECAM System Color Television Receiver

### RECOMMENDED OPERATING CONDITION

Supply voltage range.....10.0~12.5V  
 Rated supply voltage.....12V



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V <sub>cc</sub>	Supply voltage	13.5	V
P <sub>d</sub>	Power dissipation	1.25	W
T <sub>opr</sub>	Operating temperature	-20~65	°C
T <sub>stg</sub>	Storage temperature	-40~125	°C
Surge	Surge voltage resistance	200	V
Latch	Latch-up voltage resistance	300	V
V <sub>I6</sub>	Pin ⑥ voltage	0.28V <sub>cc</sub> + 6	V
I <sub>I7</sub>	Pin ⑦ input current	+6	mA
I <sub>I4</sub>	Pin ④ input current	-1.0	mA











PAL/NTSC VIDEO CHROMA DEFLECTION

**ELECTRICAL CHARACTERISTICS TEST METHOD**

**GY** Video amplifier gain

1. Test-Y output amplitude and make  $V_{CO}$  the testing value.

$$2. GY = 20 \times \log \frac{V_{CO}(mV_{P-P})}{200(mV_{P-P})} \text{ (dB)}$$

**GYMID 1 GYMAX** Contrast control characteristics-1

1.  $GY_{MID 1} = V_{CO}(V_{P-P})$

2. Test-Y output amplitude and make  $V_{C1}$  the testing value.

$$3. GY_{MAX} = 20 \times \log \frac{V_{C1}(mV_{P-P})}{V_{CO}(mV_{P-P})} \text{ (dB)}$$

**GYMIN** Contrast control characteristics-2

1. Test-Y output amplitude and make  $V_{C2}$  the testing value.

$$2. GY_{MIN} = 20 \times \log \frac{V_{C2}(mV_{P-P})}{V_{CO}(mV_{P-P})} \text{ (dB)}$$

**GYMID 2** Contrast control characteristics-3

1. Test-Y output amplitude and make  $V_{C3}$  the testing value.

$$2. GY_{MID 2} = 20 \times \log \frac{V_{C3}(mV_{P-P})}{V_{CO}(mV_{P-P})} \text{ (dB)}$$

**YTMD** Video tone control characteristics-1

1. Test-Y output amplitude and make  $V_{T0}$  the testing value.

2.  $YT_{MID} = V_{T0}(V_{P-P})$

**YTMIN** Video tone control characteristics-2

1. Test-Y output amplitude and make  $V_{T1}$  the testing value.

$$2. Y_{TMIN} = 20 \times \log \frac{V_{T1}(mV_{P-P})}{V_{T0}(mV_{P-P})} \text{ (dB)}$$

**YTMAX** Video tone control characteristics-3

1. Test-Y output amplitude and make  $V_{T2}$  the testing value.

$$2. Y_{TMAX} = 20 \times \log \frac{V_{T2}(mV_{P-P})}{V_{T0}(mV_{P-P})} \text{ (dB)}$$

**YBRTMD** Luminance control characteristics-1

1. Test-Y output DC voltage.

**YBRTMIN** Luminance control characteristics-2

1. Same as Y9

**YBRTMAX** Luminance control characteristics-3

1. Same as Y9

**Yf** Frequency characteristics

1. Test-Y output amplitude.

2. Make  $V_{f1}$  the amplitude when SG2 is input.

3. Make  $V_{f2}$  the amplitude when SG4 is input.

$$4. Y_f = 20 \times \log \frac{V_{f2}}{V_{f1}} \text{ (dB)}$$

**DG** Differential gain

1. Test-Y output DC voltage.

2. Make  $V_{G1}$  the amplitude when pin④ is set 2.4V.

3. Make  $V_{G1}$  the amplitude when pin④ is set 1.8V.

$$4. DG = \frac{|V_{G1}-V_{G2}|}{V_{G2}} \times 100 \text{ (\%)}$$

**H.BLK TH** Horizontal blanking threshold voltage

1. Apply voltage to pin④ and increase from 8V.

2. Test the voltage of pin④ when signal ceases to be output by ①A.

**GC** Chroma maximum gain

1. Test output amplitude (P-P) and make  $V_{GC}$  the testing value.

2. Input amplitude.

$$GC = 20 \times \log \frac{V_{GC} (mV_{P-P})}{\text{Input amplitude (= 7.94mV}_{P-P})} \text{ (dB)}$$

**ACC 1** ACC characteristics-1

1. Test output amplitude (P-P).

2. Make  $V_{A0}$  the testing value when SG5 0dB is input.

3. Make  $V_{A1}$  the testing value when SG5 -20dB is input.

$$4. ACC 1 = 20 \times \log \frac{V_{A1}}{V_{A0}} \text{ (dB)}$$

**ACC 2** ACC characteristics-2

1. In the same manner as in C3, make  $V_{A2}$  the testing value when SG5 +6dB is input.

$$2. ACC 2 = 20 \times \log \frac{V_{A2}}{V_{A0}} \text{ (dB)}$$

**KIL** Killer operation input

1. Gradually attenuate the level of SG5.

2. While monitoring DC voltage of pin④, input level of SG5 when voltage becomes less than 1V.

**D KIL** Killer color residual

1. Test output amplitude within 1H interval.

**CCMID 1** CCMAX color control characteristics-1

1. Test output amplitude (P-P) and make  $V_{C10}$  the testing value.

2.  $CC_{MID 1} = V_{C10} (V_{P-P})$

3. Test output amplitude (P-P) and make  $V_{C11}$  the testing value.

$$4. CC_{MAX} = 20 \times \log \frac{V_{C11}}{V_{C10}} \text{ (dB)}$$

**CCMIN** Color control characteristics-2

1. Test output amplitude (P-P) and make  $V_{C12}$  the testing value.

$$2. CC_{MIN} = 20 \times \log \frac{V_{C12}}{V_{C10}} \text{ (dB)}$$

## PAL/NTSC VIDEO CHROMA DEFLECTION

**CCMID 2** Color control characteristics-3

1. Test output amplitude (P-P) and make  $V_{C13}$  the testing value.

$$2. \text{CCMID } 2 = 20 \times \log \frac{V_{C13}}{V_{C10}} \text{ (dB)}$$

**UCMID 1** UCMAX color tracking characteristics-1

1. Test output amplitude (P-P) and make  $V_{U0}$  the testing value.

$$2. \text{UCMID } 1 = V_{U0} \text{ (V}_{P-P}\text{)}$$

3. Test output amplitude (P-P) and make  $V_{U1}$  the testing value.

$$4. \text{UCMAX} = 20 \times \log \frac{V_{U1}}{V_{U0}} \text{ (dB)}$$

**UCMIN** Color tracking characteristics-2

1. Test output amplitude (P-P) and make  $V_{U2}$  the testing value.

$$2. \text{UCMIN} = 20 \times \log \frac{V_{U2}}{V_{U0}} \text{ (dB)}$$

**UCMID 2** Color tracking characteristics-3

1. Test output amplitude (P-P) and make  $V_{U3}$  the testing value.

$$2. \text{UCMID} = 20 \times \log \frac{V_{U3}}{V_{U0}} \text{ (dB)}$$

**APC 1** APC pull-in range-1

1. Set so that the frequency of SG6 is less than 4.433MHz and pin ② is Lo.
2. Gradually increase the frequency of SG6.
3. Test the frequency when the voltage of pin ② changes from Lo to Hi and make  $F_{A\mu}$  the testing value.
4.  $\text{APC } 1 = 4433619(\text{Hz}) - F_{A\mu}(\text{Hz})$

**APC 2** APC pull-in range-2

1. Set so that the frequency of SG6 is more than 4.434MHz and pin ② is Lo.
2. Gradually decrease the frequency of SG6.
3. Test the frequency when the voltage of pin ② changes from Lo to Hi and make  $F_{Ad}$  the testing value.
4.  $\text{APC } 2 = F_{Ad}(\text{Hz}) - 4433619(\text{Hz})$

**DDC** Demodulated output DC voltage

1. Test DC voltage at ①A, ②A, and ③A.

**D OFF** Demodulated output DC offset

1. Calculate each voltage difference of ①A②A, ②A③A, ③A①A from the testing value of C15.

**RB** Demodulation ratio-1

1. Test output amplitude and make DR-Y testing value.

$$2. \text{RB} = \frac{\text{DR-Y}}{\text{DB-Y(Testing value at C18)}} \text{ (dB)}$$

**DB** Demodulation ratio-2

1. Test output amplitude and make DG-Y the testing value.

$$2. \text{GB} = \frac{\text{DG-Y}}{\text{DB-Y(Testing value at C18)}} \text{ (dB)}$$

**DDH** Demodulated output 1H level difference

1. Test both AC, DC for each 1H level difference.

**CL** Demodulated output carrier leak

1. Test output carrier element for ①A, ②A, and ③A.

**VN** NTSC operation control voltage

1. Gradually decrease voltage of ③A from the area of 8V.
2. Test the ③A voltage when signal ceases to be output by ①A.

**NTSC R/B** Demodulation ratio (NTSC)-1

1. Test output amplitude and make NTSC<sub>R</sub> the testing value.

$$2. \text{NTSC R/B} = \frac{\text{NTSC}_R}{\text{NTSC}_B(\text{Testing value at C25})}$$

**NTSC G/B** Demodulation ratio (NTSC)-2

1. Test output amplitude and make NTSC<sub>R</sub> the testing value.

$$2. \text{NTSC R/B} = \frac{\text{NTSC}_R}{\text{NTSC}_B(\text{Testing value at C25})}$$

**V/P/N** PAL/NTSC demodulated output DC voltage difference

1. Test the difference in DC voltage when (S34) is on and when it is OFF.

**SS** Service switch operation

1. No output signal from ④.
2. No vertical sync pulse from ⑤.
3. Voltage of ⑥ drops below 1V.
4. Check 1, 2, and 3.

**DBW** Demodulated output bandwidth

1. Set frequency of SG8 to 4.5MHz, and test output amplitude of ①, ② and ③.
2. Gradually increase the frequency of SG8.
3. Test output frequency of ①, ②, and ③ when output amplitude is 3dB less than when 4.5MHz is input.

**CD** Chroma input dynamic range

1. Increase the level of SG5 and test the input amplitude when output become distorted.

**RYP, GYP** Pal demodulated phase angle

1. Make R-Y-P the phase difference of ①A, ②A.
2. Make G-Y-P the phase difference of ①A, ③A.

**RYN, GYN** NTSC Demodulated phase angle

1. Make R-Y-N the phase difference of ①A, ②A.
2. Make G-Y-N the phase difference of ①A, ③A.

PAL/NTSC VIDEO CHROMA DEFLECTION

**TMIN, TMAX** NTSC Tint

1. Set oscilloscope to X-Y. Connect (A) to X and (2A) to Y.
2. Open (34A) and set SG6 frequency to 4.433619MHz.
3. At this time the oscilloscope waveform is shown as 180°.
4. Make TMIN the remainder of subtracting 180° from the angle when (34A) was set to 4V.
5. Make TMAX the remainder of subtracting 180° from the angle when (34A) was set to 1V.

**V9MIN** Horizontal oscillator starting voltage

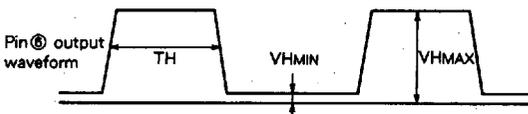
1. Increase (VCC) from 0V.
2. Test (VCC) voltage where the output waveform cycle of pin (6) is approx 64μs.

**F PHL, F PHH** Horizontal pull-in range-1

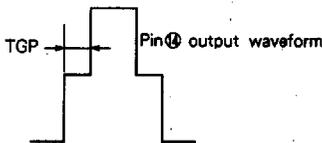
1. Decrease the frequency of input signal so that the SGB input signal and pin (6) output waveform are not synchronized.
2. Increase the frequency of SGB.
3. Test the SGB frequency when SGB and pin (6) output waveforms become synchronized and make FL1 the testing value.
4. (Testing value at J3)
5. Test the upper side pull-in the same manner and make FH1 the SGB frequency when the two become synchronized.
6. (Testing value at J3)

**TH** Horizontal output pulse amplitude

**VH MIN, VH MAX** Horizontal output voltage



**TPG** Burst gate pulse position



**FPV50** Vertical pull-in range 50(Hz)

1. Increase the frequency of input signal so that the SGc input signal and pin (15) output waveform are not synchronized.
2. Decrease the frequency of SGc and test the SGc frequency when SGc and the output waveform of pin (15) become synchronized.

**FPV60** Vertical pull-in range 60(Hz)

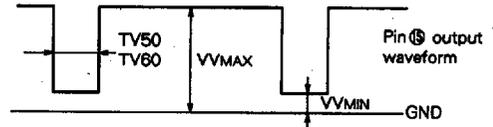
1. Same as J12.

**TV50** Vertical output pulse amplitude 50(Hz)

**TV60** Vertical output pulse amplitude 60(Hz)

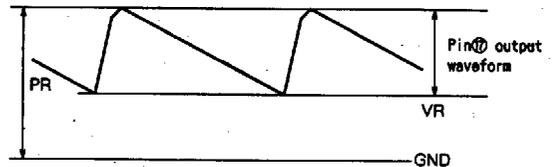
**VVMAX** Vertical output maximum voltage

**VVMIN** Vertical output minimum voltage



**PR** Ramp peak voltage

**VR** Ramp amplitude



**Gvw** Vertical open loop gain

1. Test the output amplitude of pin (15) and make Vvo the testing value.

$$2. Gvw = 20 \times \log \frac{Vvo(mV_{P-P})}{\text{Input amplitude}(= 50mV_{P-P})} \text{ (dB)}$$

**Iss** Sync separation input sensitivity current

1. Increase is from 0mA.
2. Test is when burst gate pulse ceases to be output by (14).

**Tsep 1** Burst gate pulse timing-1

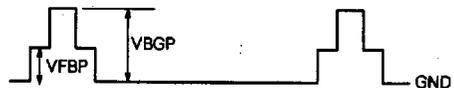
1. Test the time from SGa rise to burst gate pulse rise.

**Tsep 2** Burst gate pulse timing-2

1. Test burst gate pulse amplitude.

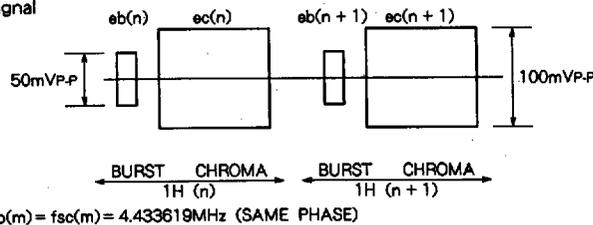
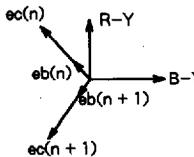
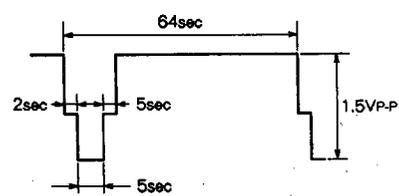
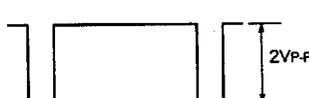
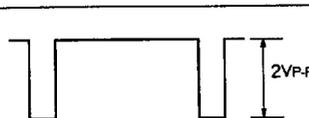
**VFBP** Flyback pulse clamp voltage

**VGBP** Burst gate pulse voltage



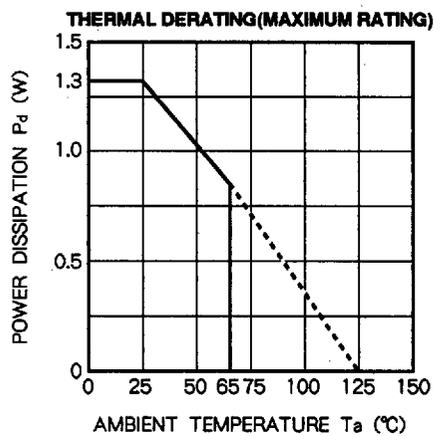
PAL/NTSC VIDEO CHROMA DEFLECTION

INPUT SIGNAL

SG. No.	Signal		
SG 1	100kHz	CW	3V <sub>P-P</sub>
SG 2	100kHz	CW	200mV <sub>P-P</sub>
SG 3	2MHz	CW	200mV <sub>P-P</sub>
SG 4	5MHz	CW	200mV <sub>P-P</sub>
SG 5	<p>PAL simple chroma signal</p>  <p> <math>f_{sb}(m) = f_{sc}(m) = 4.433619\text{MHz}</math> (SAME PHASE)         </p> <p>The phase correlation between the about signal is outlined in the figure on the right. The phase correlation with burst of <math>ec(n)</math> and <math>ec(n+1)</math> does not always have to be as shown in the figure on the right, and in particular must be adjustable according to conditions when testing phase correlation.</p> 		
SG 6	With PAL simple chroma signals for SG5, the phase of burst and chroma signals should be the same and the frequency should be adjustable.		
SG 7	4.42MHz	CW	0.2~0.5V <sub>P-P</sub>
SG 8	4~6MHz	CW	
SG 9	$f_{sb}$ (Burst) = 4.433619MHz, $f_{sc}$ (Chroma) = 4.53MHz at SG5.		
SG a	<p>Input for sync separation should be APL 100% standard combined image signal 1.5V<sub>P-P</sub> for PAL system such as illustrated by the figure on the right.</p> 		
SG b	 <p>Duty 90%</p>		
SG c	 <p>Duty 95%</p>		
SG d	2kHz, CW ; 500mV <sub>P-P</sub> = 0dB		



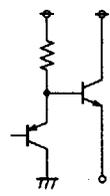
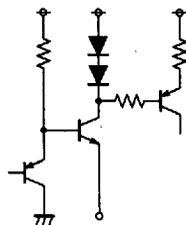
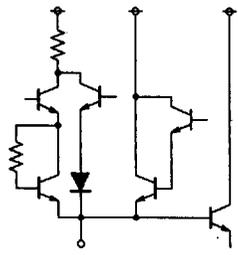
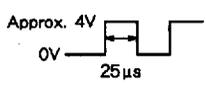
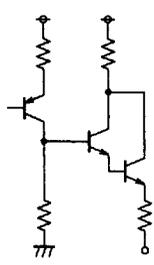
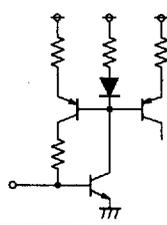
## TYPICAL CHARACTERISTICS





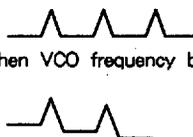
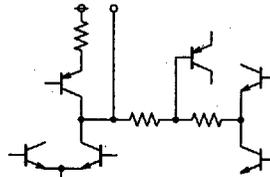
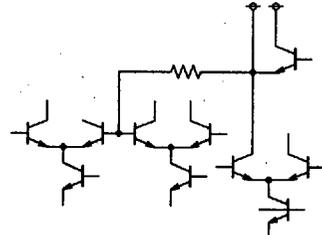
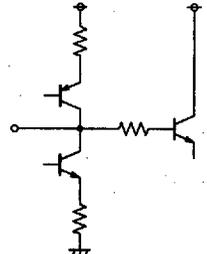
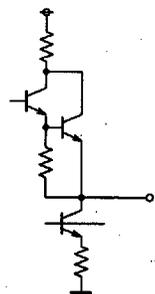
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
①	B-Y OUTPUT	<ul style="list-style-type: none"> <li>• Chroma output</li> <li>B-Y</li> <li>R-Y</li> </ul>		6.4
②	R-Y OUTPUT			
③	G-Y OUTPUT	<ul style="list-style-type: none"> <li>• Chroma output</li> <li>G-Y</li> <li>• If color tracking switch external resistor (emitter resistor) is removed, color tracking is ineffectual.</li> </ul>		6.4
④	-Y OUTPUT	<ul style="list-style-type: none"> <li>• -Y output</li> <li>• Horizontal blanking input</li> </ul>		-
⑤	GND	-	-	0
⑥	HORIZONTAL OUTPUT	<p>Approx. 4V</p>  <p>0V</p> <p>25μs</p> <p>Horizontal pre-driver output</p>		-
⑦	X-RAY PROTECTOR	X-RAY protector is actuated when pin voltage exceeds approx. 0.75V.		-

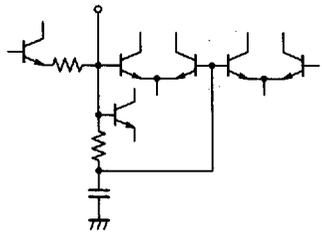
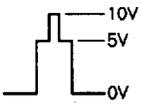
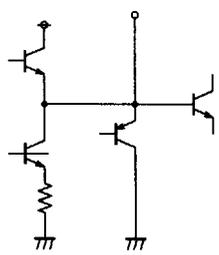
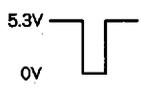
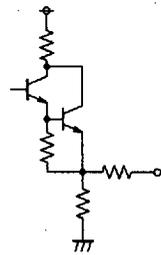
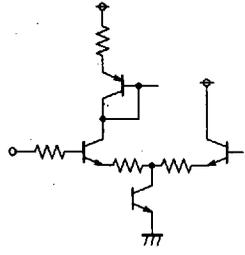
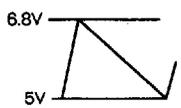
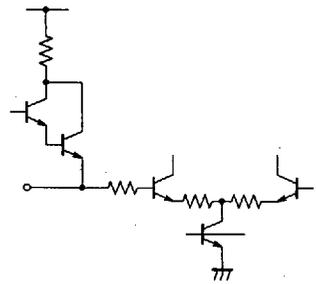
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑧	AFC1 FILTER	 <p>When VCO frequency becomes high</p> <p>Filter voltage decreases causing VCO frequency to drop. Operates oppositely when frequency become high.</p>		6.6
⑨	Vcc H	Built-in regulator	-	10
⑩	HORIZONTAL RAMP	 <p>Generates horizontal ramp. Horizontal output pulse is created according to this ramp.</p>		-
⑪	COINCIDENCE DETECTION FILTER	High when horizontal SYNC and horizontal output are synchronized, low when not synchronized.		Low 0.2 High 9.1
⑫	HORIZONTAL OSCILLATOR OUTPUT	 <p>f = approx. 500kHz Output to external phase shifter.</p>		9.5

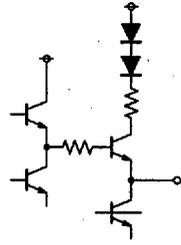
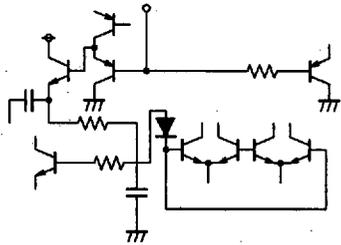
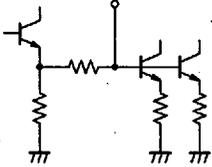
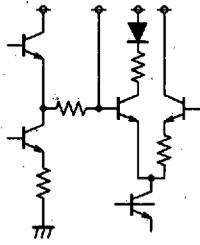
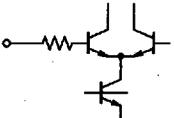
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
13	HORIZONTAL OSCILLATOR INPUT	 f = approx. 500kHz Output to external phase shifter.		5.2
14	F.B.P. INPUT/ B.G.P. OUTPUT	4.3μs  B.G.P. and f.b.p. output as sandcastle.		-
15	VERTICAL OUTPUT	 5.3V 0V		-
16	VERTICAL RETURN	AC/DC return input pin		-
17	VERTICAL RAMP	 6.8V 5V Vertical ramp generation		-

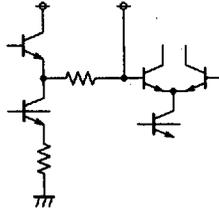
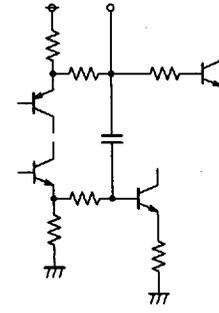
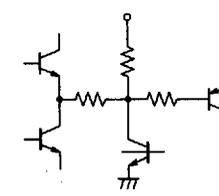
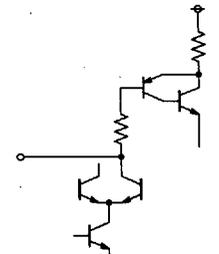
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑮	SYNC SEPARATION INPUT	Sync separation of emitter input		8.4
⑯	PICTURE QUALITY CONTROL/ PICTURE MUTING SWITCH	<ul style="list-style-type: none"> <li>Picture quality control</li> <li>High-pass increases as pin voltage is decreased.</li> <li>Picture muting</li> <li>If voltage is less than 2V, picture muting is actuated and -Y output become BLK level.</li> <li>Built-in buffer</li> </ul>		-
⑳	Y INPUT	Y signal input		1.3
㉑	PEDESTAL CLAMP	Pedestal DC voltage of -Y output is determined by this clamp voltage.		2
㉒	LUMINANCE CONTROL	<ul style="list-style-type: none"> <li>Luminance control</li> <li>Become brighter as voltage is increased.</li> </ul>		-

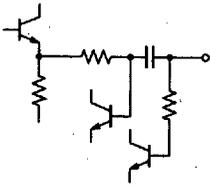
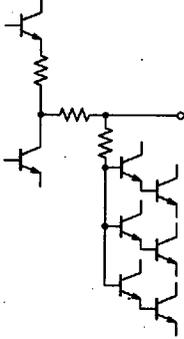
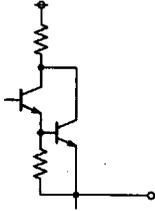
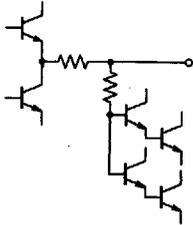
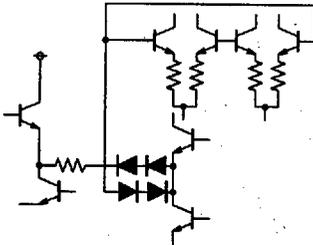
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑫	DC PLAYBACK	DC playback ratio can be changed by external CR. 100% when open.		-
⑭	Vcc	-	-	11
⑮	COLOR SIGNAL INPUT 50/60 SW	<ul style="list-style-type: none"> <li>• Chroma input</li> <li>• 50/60 switching</li> </ul> Vertical countdown toggles between 50Hz and 60Hz. When voltage exceeds 5.6V, toggles to 60Hz.		2.7 -
⑯	COLOR SATURATION CONTROL	Changes amplitude of chroma output.		-
⑰	PEAK ACC FILTER	Gain of chroma amp is controlled by this filter in order to maintain a constant chroma amplitude.		-

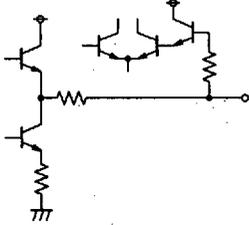
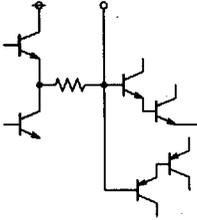
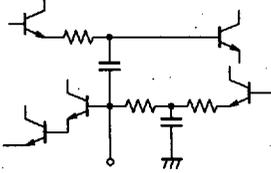
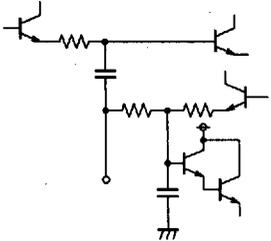
PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
②	CONTRAST CONTROL/ BURST CHEANING	Burst cleaning Coil connection contrast control Changes amplitude of -Y output. Amplitude increases as voltage is increased.		-
③	ACC/KILLER (1) / SERVICE SWITCH	Sync acc/killer filter ACC and killer are operated according to voltage differential between this pin and pin④. When this pin is connected to GND, the service switch is ON. (Vertical stop and cotrast MIN, killer ON.)		7.3
④	CHROM OUTPUT	PAL system ACC chroma signals are output. NTSC system Low DC chroma signals are output.		7.1 4.2
⑤	ACC/KILLER FILTER (2)	Sync acc/killer filter ACC and killer are operated according to voltage differential between this pin and pin③.		7.3
⑥	APC FILTER	Chroma VCO phase is controlled by this voltage in order to check burst.		9.1

PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION OF PIN (Cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑤	CHROMA VCO	Generates carrier for chroma.		8
④	IDENT FILTER/ NTSC TINT CONTROL	PAL system Functions as ident filter. When voltage drops below reference voltage, F.F. is stopped. NTSC system (less than 5V) Tint control is carried out at 2~4V. If NTSC switch is less than 5V, switches to NTSC mode.		8
⑥	B-Y INPUT	PAL system Synthesized B-Y chroma signal input		6
⑦	R-Y INPUT	PAL system Synthesized R-Y chroma signal input.		2