FUJITSU

CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH MULTI I/O PORT

MB88520 SERIES

TM318-B871: January 1987

CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH MULTI I/O PORT

The Fujitsu MB88520 series CMOS single-chip 4-bit microcomputer family is a upgrade version of the MB88500 series, which designed based on the MB88500 series 4-bit microcomputer architecture and added multi I/O port.

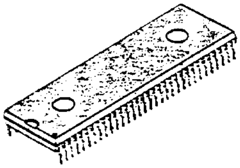
The MB88520 series consists of MB88521, MB88522, MB88523, and MB88525. This series contains max. 4K by 8-bit mask ROM (program memory), 256 by 4 bit static RAM (data memory), a 57 I/O lines, (including serial port), an 8-bit timer/counter, and a clock generator.

They are fabricated by silicon-gate CMOS process, and packaged in an 64-pin plastic shrink DIP (suffix -PSH) or 64-pin plastic flat package (suffix -PF). They operate with a single +5V power supply over the temperature range of -30°C to +70°C. And the instruction execution time is 2.0 µs min. at a 6 MHz crystal with a prescaler.

CMOS technology allows the device to operate with low power dissipation (6 mA max. at fc=1 MHz), and further the standby function (if implemented) enables data retention with lower current (15 µA max. at V_{CC}=6.0 V).

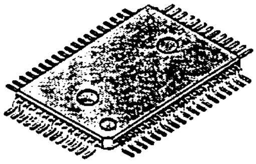
For user's development of the MB88520 series based system, Fujitsu provides the MB88400/500 cross-assemblers and host-emulator which run on the CP/M-86 or PC-DOS machines (cross-assembler also run on the Intellec series III MDS), and the MB2115 series evaluation board system. Further, MB88528 for MB88521/MB88523/MB8525 and MB88PG522 for MB88522 piggyback EPROM evaluation device which have external 8K x 8 bit EPROM (MBM27C64). These development tools enables users to minimize their development time and cost.

MB88521-PSH
MB88522-PSH
MB88523-PSH
MB88525-PSH



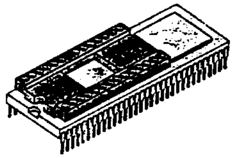
64-PIN PLASTIC SHRINK DIP
(DIP-64P-M01)

MB88521-PF
MB88523-PF



64-PIN PLASTIC FLAT PACKAGE
(FPT-64P-M01)

MB88528-CSH
MB88PG522-CSH



64-PIN CERAMIC MODULE
(MDP-64C-P01)

FEATURES

- CMOS Single Chip 4-bit Microcomputer

- Program Memory:
  - o MB88521, MB88522, MB88525: 4K x 8-bit mask ROM
  - o MB88523 : 2K x 8-bit mask ROM

- Data Memory:
  - o 256 x 4-bit data memory (Static RAM)

- Three Selectable Output Port Types for O-, P-, R-, E-Ports Circuits, Every 4-bit Port With Mask Option:
  - o Standard open-drain
  - o Standard pull-up
  - o 12V-interface open-drain (P-Port only)

- 57 I/O Lines:
  - o K-Port: A 4-bit parallel input only port
  - o P-Port: A 4-bit parallel output only port
  - o O-Port: A 4-bit parallel output only port
  - o R-Port: Four 4-bit parallel or 16 individual input/output
  - o E-Port: Six 4-bit parallel I/O or 24 individual output:
  - o C-Port: Serial I/O, external interrupt input, timer/counter input, and timing output

- Square Wave Output by Timer/Counter Overflow to $\overline{\text{SC}}/\overline{\text{TO}}$ Pin.

- 8-bit Programmable Timer/Counter with Auto-loading Function/Two Clock Modes:
  - o Internal (Timer)
  - o External (Counter)

- Software Selectable Serial I/O with Output Latch:
  - o MB88521, MB88522, MB88523 : 4-bit serial buffer
  - o MB88525 : Software selectable 4/8-bit serial buffer

- Three Selectable Serial I/O Clock Modes:
  - o Internal clock
  - o External clock
  - o Software clock

- On-chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC-network or external clock drive

- Mask Option Divided-by-two Clock Prescaler for Expanding Clock Range

- Single Level Four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty

- 8-nesting Levels for Subroutine Call

FEATURES (Continued)

- Instruction Set : Upward compatible with the MB88500 series
  - Number of instructions : 80
  - Instruction length/cycle: 1, 2, or 3 byte(s)/1 , 2, or 3 cycle
  - Execution time : 2.0 µs min. at 6 MHz clock with prescaler

- On-chip Power-on Reset Circuit

- Mask Option Low Power Standby Function: Software initiation and hardware release

- Two Selectable Output Port (P-port) Level During Reset with Mask Option:
  - High level
  - Low level

- Two Selectable Output During Standby with Mask Option:
  - Hold
  - High impedance

- Two Software Selectable Oscillation States During Standby:
  - Idle
  - Stop

- Mask Option Standby Off Reset

- Mask Option Watch-dog Timer Function

- Low Power Dissipation:
  - 6 mA at fc=1 MHz max. (Active mode)
  - 15 µA at fc=0 MHz max. (Standby mode)

- Single +5V Power Supply
  - 4.5 V to 5.5 V (Active mode)
  - 3.5 V to 6.0 V (Standby mode)

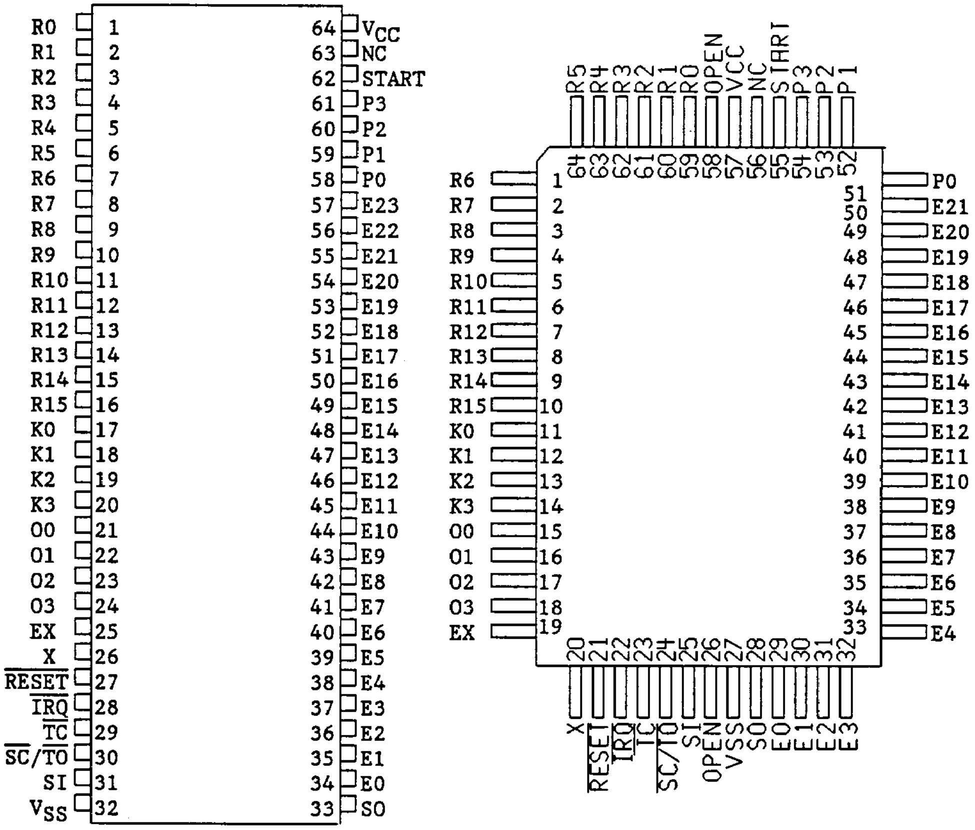
- Wide Operation Temperature Range: T_A= -30 °C to +70 °C

- Silicon Gate CMOS Technology

- Two Type Package:
  - 64-pin plastic shrink DIP : Suffix -PSH (MB88521, MB88522, MB88523, MB88525)
  - 64-pin plastic flat package: Suffix -PF (MB88521, MB88523)

- Powerful Development Support:
  - CP/M-86, PC-DOS, or Intellec series III MDS cross assemblers (SM07415-A012/SM05215-A010/SMXXXX-XXXX)
  - CP/M-86 or PC-DOS host-emulator software for monitoring evaluation board and symbolic debugging (SM07415-G022/SMXXXX-XXXX)
  - MB2115 evaluation board for software debugging
  - MB88528 for MB88521/MB88523/MB88525 and MB88PG522 for MB88522 CMOS piggyback EPROM evaluation

Fig. 1: PIN ASSIGNMENT



64-pin plastic shirnk DIP
(Suffix -PSH)
MB88521-PSH
MB88522-PSH
MB88523-PSH
MB88525-PSH

64-pin plastic flat package
(Suffix -PF)

MB88521-PF
MB88523-PF

Fig. 2: MB88521, MB88523, AND MB88525 LOGIC SYMBOL

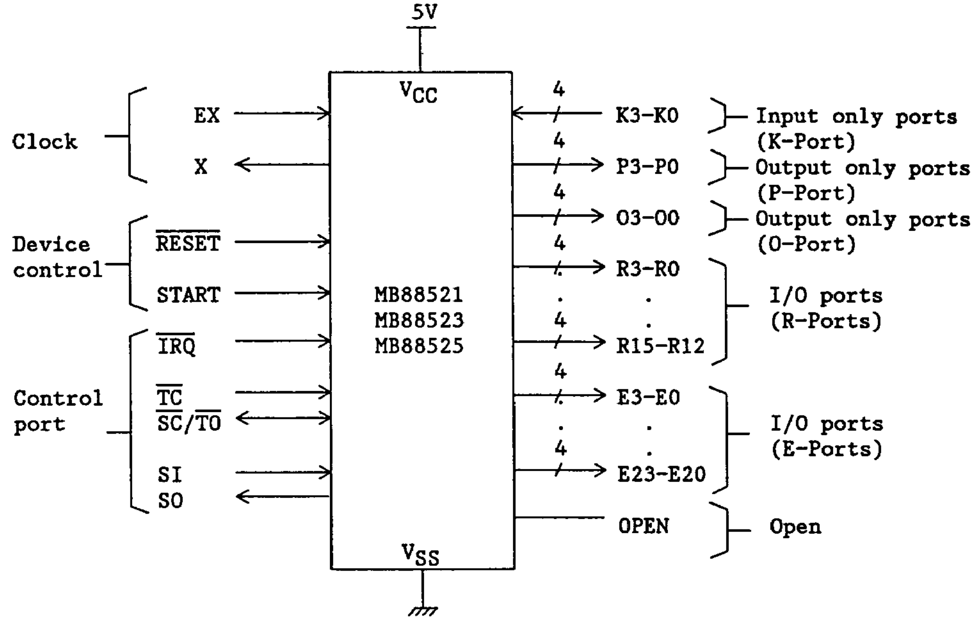


Fig. 3: MB88522 LOGIC SYMBOL

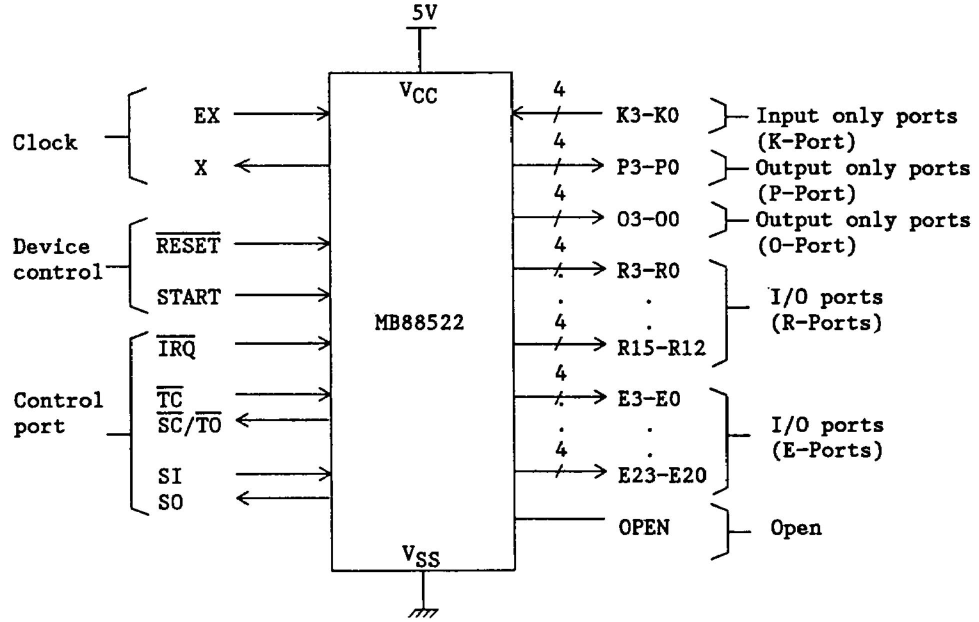
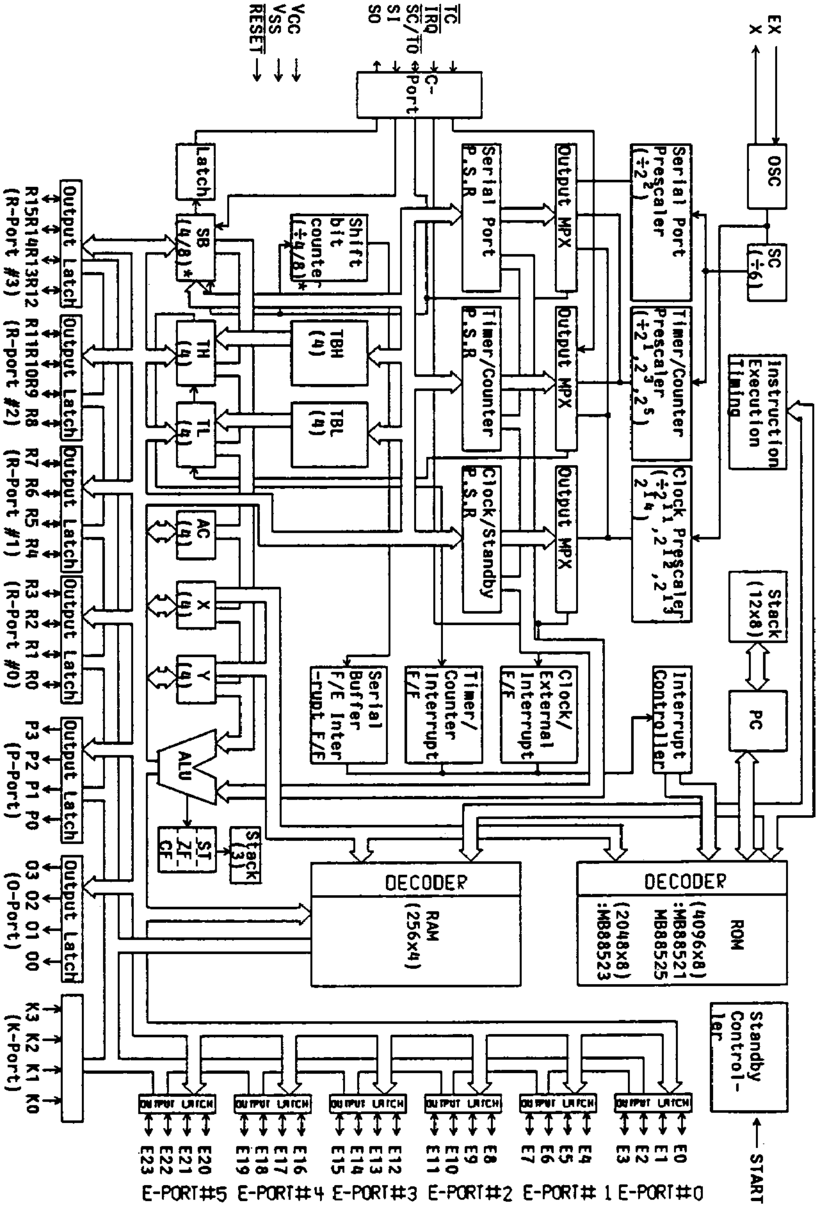


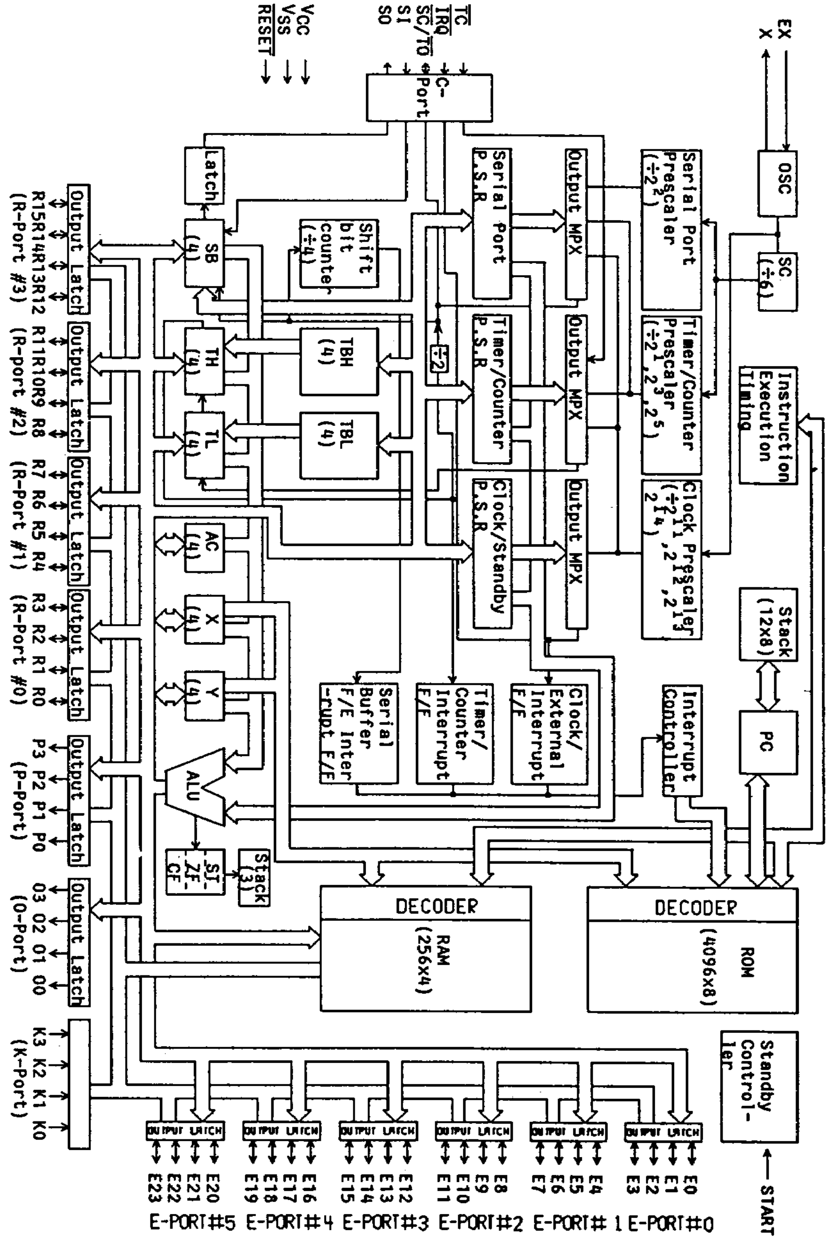
Fig. 4: MB88521, MB88523, AND MB88525 BLOCK DIAGRAM



* MB88521/MB88523 is 4 bit

P.S.R: Prescaler Select Register

Fig. 5: MB88522 BLOCK DIAGRAM



P.S.R: Prescaler Select Register

PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88520 Series.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	64	-	+5V DC power supply pin.
V_{SS}	32	-	Ground pin.
• Clock			
EX	25	I	**Oscillator Input**: Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ ceramic oscillator is selected, and a hysteresis input when the RC-network oscillation is selected.
X	26	O	**Oscillator Output**: Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the X pin should be left open.
• Device Control			
$\overline{\text{RESET}}$	27	I/O	**Reset**: This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{\text{RESET}}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{\text{RESET}}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{\text{RESET}}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on. This pin is a hysteresis input with an internal pull-up resistor. An external capacitor from the $\overline{\text{RESET}}$ pin to the VSS pin (and the internal pull-up resistor), whose time constant should be greator than the reset time required (12 clock periods) composes the external reset circuit. Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the $\overline{\text{RESET}}$ pin, and then automatically returns high after it has passed 2^{18} clock periodes since the oscillator starts by power on.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
$\overline{\text{RESET}}$	27	I/O	This pin is a hysteresis input with an internal pull-up resistor.
START	62	I	**Start**: A standby release input to the internal standby control and status registers that control and monitor the on-chip standby control circuit. A high level on the START pin during the stanbdy mode sets te standby release flag (STF) in the stanbdy status register, resets the standby enable flag (STBE) in the standby control registor, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the VCC voltage must return to the active operation range (4.5V to 5.5V) when the battery backup is used. Also, the START pin must be low before the standby mode is initiated. The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the standby status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8). This pin is a hysteresis input with an internal pull-down resistor.
• C-Port			
$\overline{\text{IRQ}}$	28	I	**Interrupt Request**: A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{\text{IRQ}}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{\text{IRQ}}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{\text{IRQ}}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pull-up resistor.
$\overline{\text{TC}}$	29	I	**Timer/Counter**: An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{\text{TC}}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B).

Table 1: **PIN DESCRIPTION** (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
$\overline{TC}$	29	I	Also, the TC pin state (logical level), which is reflected in the timer/counter input flag (TCF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter) mode, is testable by reading the prescaler select register using IN instruciton (with Y = B). (When $\overline{TC}$ = L, TCF = 1; otherwise TCF = 0.) This pin is inactive as a count clok input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pull-up resistor.
$\overline{SC}/\overline{TO}$	30	I/O	**Shift Clock/Timing Output**: One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
		I	$\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selcted or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization.
		O	(MB88521, MB88523, MB88525) $\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. (MB88522) $\overline{TO}$: Sqare wave output: By enabled the EN 10 instruciton, When timer/counter overflow, invert the output level. MB88522 don't have synchronous timing output. This pin is a hysteresis input with an internal pull-up resistor

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
SI	31	I	**Serial Data Input**: Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shift clock shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data iput flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instrution (with Y = A).
SO	33	O	**Serial Data Output**: Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appeares on the SO pin. This pin is a CMOS pull up output, and is set high by reset.
• I/O Ports			
K3-K0	20-17	I	**K-Port**: A 4-bit parallel non-latched input-only port. K0 is LSB. 4-bit data on K-Port is input into the accumulator by INK instruction. These pins are internally pulled up.
P3-P0	61-58	O	**P-Port**: A 4-bit parallel latched output-only port. P0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTP instruction. Refer to table 4 User mask option for available making option.
O3-O0	24-21	O	**O-Port**: A 4-bit parallel latched output-only port. O0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTO instruction. Refer to table 4 User mask option for available making option.
• I/O Ports (Continued)			
R3 -R0, R7 -R4, R11-R8, R15-R12	4- 1, 8- 5, 12- 9, 16-13	I/O	**R-Port**: This port functions as four 4-bit parallel input (non-latched)/output (latched) port, or 16 individual input (non-latched)/output (latched) lines, depending on instructions.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Ports (Continued)			
R3 -R0, R7 -R4, R11-R8, R15-R12	4- 1, 8- 5, 12- 9, 16-13	I/O	Parallel I/O: Each port is named as R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and indirectly addressed by the Y-register. A 4-bit data on an addressed port is input into the accumulator by IN instruction. (Before IN instruction, the addressed port must be setup to "1" (input mode).) A 4-bit data in the accumulator is output onto an addressed port of R-Port #0 to #3 by OUT instruction. Individual I/O: Each line of R15 to R0 is indirectly addressed by the Y-register, and addressed line is individually set/reset by SETR/RSTR instruction, and further each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. All lines are testable using TSTR instruction, and further each line of R-Port #2 (R11-R8) is directly testable by TSTD instruction. (Before TSTR and TSTD instructions, the addressed line must be setup to "1" (input mode).) Refer to table 4 User mask option for available making option.
E3 -E0, E7 -E4, E11-E8, E15-E12, E19-E16, E23-E20	37-34, 41-38, 45-42, 49-46, 53-50, 57-54	I/O	**E-Ports:** This functions as six 4-bit parallel input (non-latched)/output (latched) port, or 24 individual output (latched) lines. Parallel I/O: Each port is named as E-Port #0 (E3-E0), E-Port #1 (E7-E4) ... E-Port #5 (E57-E54), and indirectly addressed by Y-resister. A 4-bit data on an addressed port is input into the accumulator by INX (before INX instruction, the addressed port must be setup to "1" (input mode).)instruction. A 4-bit data in the accumulator is output onto an addressed port of E-Port #0 to #6 by OUTX instruction. Individual output: Each line of E23 to E0 can be individually outputs by combined of ANDX, ORX, and OUTX instruction. Refer to table 4 User mask option for available making option.
OPEN	63	-	**Open:** This pin should not to be connect.

DIFFERENCES BETWEEN MB88500 SERIES AND MB88520 SERIES

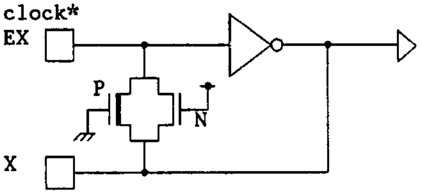
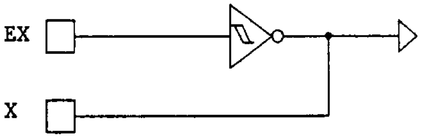
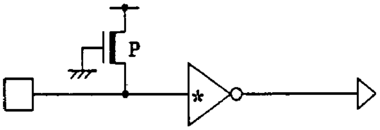
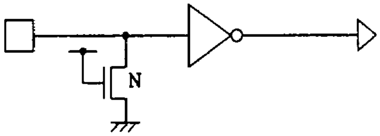
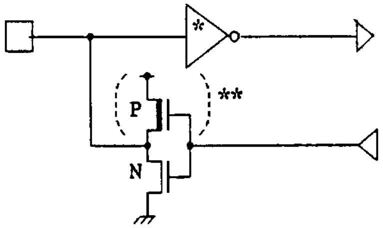
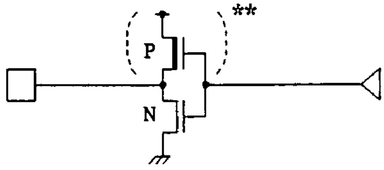
Table 2: DIFFERENCES BETWEEN MB88501 AND MB88520 SERIES

Item \ Device	MB88501	MB88520 series
Clock -oscillation range	· 0.5 MHz to 2 MHz (Without prescaler) 1 MHz to 4.19 MHz (With prescaler)	· 0.5 MHz to 3 MHz (Without prescaler) 1 MHz to 6 MHz (With prescaler)
-Min. instruction cycle	· 2.86 µs using 4.19 MHz with prescaler	· 2.0 µs using 6 MHz with prescaler
-Clock output	· No	· Yes
ROM size	· 4K x 8 bits	· 4K x 8 bits: MB88521/22/25 · 2K x 8 bits: MB88523
RAM size	· 192 x 4 bits	· 256 x 4 bits
Serial fuffer	· 4 bits	· 4 bits: MB88521/22/25 · software selectable 4/8 bits: MB88525
I/O port:		
Total I/O Port	· 37	· 57
-O-Port	· 8 bits x 1	· 4 bits x 1
-P-Port	· 4 bits x 1	· 4 bits x 1
-K-Port	· 4 bits x 1	· 4 bits x 1
-R-Port	· 4 bits x 4	· 4 bits x 4
-E-Port	· No	· 4 bits x 6
-C-Port	· 5	· 5
Output PLA	· Yes	· No
Low voltage reset function	· Yes	· No
Number of instructions	· 75	· 80
Package	· 42 Pin plastic standard DIP · 42 pin plastic shrink DIP · 48 pin plastic flat pack	· 64 pin plastic shrink DIP · 64 pin plastic flat pack
Members	· MB88501-P/-PSH/-PF · MB88503-P/-PSH/-PF · MB88505-P/PSH/-PF A- and L-versions are available for each part above.	· MB88521-PSH/-PF · MB88522-PSH · MB88523-PSH/-PF · MB88525-PSH

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and all output-only and input/output pins except O-, P-, R-, and E-Ports have push-pull output buffer (standard pull-up). O-, R- and E-Ports can have push-pull (standard pull-up) or open-drain (standard) buffer, further P-Port can have 12V interface open-drain using mask option.

Table 3: INPUT/OUTPUT CIRCUIT

<table>
<tr><th>Pin</th><th>Circuit</th><th>Remarks</th></tr>
<tr><td>EX
X</td><td>• Crystal/Ceramic OSC or external clock*
 </td><td>1. Non-hysteresis inverter
2. Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V)
* When only external clock drive is used, we recommend RC-network OSC.</td></tr>
<tr><td></td><td>• RC-network OSC or external clock*
 </td><td>1. Hysteresis inverter
2. Without feedback resistor
* When only external clock drive is used, we recommend RC-network OSC.</td></tr>
<tr><td>$\overline{IRQ}$,
$\overline{TC}$,
SI,
K-Port</td><td>• Input only-pin
 </td><td>• Input pull-up resistor (P-ch. Tr.): Approx. 300kΩ typ. (at V_{CC}=5V)
* Hysteresis inverter for $\overline{IRQ}$, $\overline{TC}$</td></tr>
<tr><td>START</td><td> </td><td>• Input pull-down resistor (N-ch. Tr.):Approx. 300kΩ typ. at (V_{CC}=5V)</td></tr>
<tr><td>$\overline{RESET}$,*
$\overline{SC}/\overline{TO}$,*
R-Port **
E-Port **</td><td>• Input/Output Pin
 </td><td rowspan="2">• Output pull-up resistor (P-ch. Tr.):
$\overline{RESET}$: Approx. 300kΩ typ.
$\overline{SC}/\overline{TO}$: Approx. 10kΩ typ. (at V_{CC}=5V)
* Hysteresis inverter for $\overline{RESET}$, $\overline{SC}/\overline{TO}$
• Output port options for O-, P-, and R-Ports
1: Standard pull-up: Pull-up resistor (P-ch. Tr.): Approx. 10kΩ typ. (at V_{CC}=5V)
**2: Standard open-drain: Without P-ch. pull-up resistor
**3: 12V interface open-drain: Without P-ch. pull-up resistor(P-Port)</td></tr>
<tr><td>SO,
P-Port,**
O-Port **</td><td>• Output-Only Pin
 </td></tr>
</table>

USER MASK OPTIONS

The MB88520 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: MB88520 SERIES USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock prescaler	CLK	No	0	f_C=0.5 MHz to 3.0 MHz
		Yes	1	f_C=1.0 MHz to 6.0 MHz
Oscillation circuit	OSC	Crystal/Ceramic OSC or external clock	0	When only external clock drive is use, we recommend RC-network oscillator.
		RC-network OSC	1	Recommend a without clock prescaler.
Port scramble		No	0	
		Yes	1	Port scramble is appointed every 4-bit.
Output port (R-, E-Port) type	PORT	Standard open-drain	L	
		Standard pull-up	M	
		12V interface open-drain	K	P-Port only
Output port level during reset	RST	High Level	0	
		Low Level	1	P-Port only
Standby function	STBY	No	0	
		Yes	1	
Output port state during standby	STATE	Hold	0	
		High-Z	1	
Standby off reset function	SOR	No	0	
		Yes	1	
Watch dog timer	WDR	No	0	
		Yes	1	

Table 4: MB88520 SERIES USER MASK OPTIONS (Continued)

When port scramble selected, output port circuit option table.

PIN NO.	PIN NAME	OUTPUT PORT OPTION
1 to 4	R0 to R3	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
5 to 8	R4 to R7	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
9 to 12	R8 to R11	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
13 to 16	R12 to R15	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
21 to 24	O0 to O3	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
58 to 61	P0 to P3	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP ☐ 12V-INTERFACE OPEN-DRAIN
34 to 37	E0 to E3	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
38 to 41	E4 to E7	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
42 to 45	E8 to E11	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
46 to 49	E12 to E15	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
50 to 53	E16 to E19	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP
54 to 57	E20 to E23	☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP

NOTES ON OPERATION

- **Latch-up Prevention**

  Latch-up may occur in CMOS devices when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins. If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**

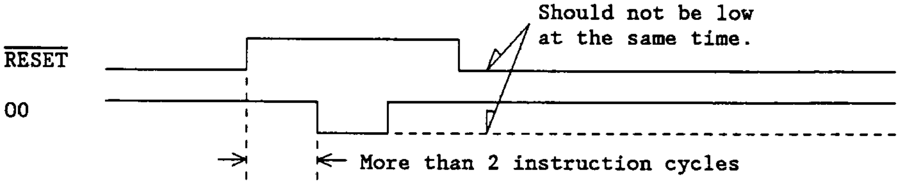
  Unused input pins should be externaly pulled up or down with resistors because such unused input pins may cause some malfunction if they are left open. (However, the X pin should be open when an external clock oscillator is used.)

- **Special Function of 00 Pin**

  The 00 pin has another function as a test terminal, in addition to its normal function R-Port. If the 00 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the 00 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the 00 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance if left floating.

  At least 2 instruction cycles are required to change R12 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **External Capacitors For Crystal Oscillation**

  Fig. 8 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

  The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

- **Supply Voltage**

  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:

  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88520 series instruction set includes 80 instructions, 83% of which are single-byte and single-cycle, 13% two-byte two-cycle, 1% two byte three-cycle, and 3% three-byte and three-cycle. The MB88520 series instruction set is exactly the same as the MB88520 series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 5 and 6 summarize the MB88520 series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status			Byte/ Cycle	Operation
			ZF	CF	ST		
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	4-bit mode: AC←(SB_L), 8-bit mode: AC←(SB_L), X←(SB_H) *4
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)⇄(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)⇄{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)⇄{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ⇄{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LXID	3D90-3D9F*	↕	·	·	2/2	X←imm; imm=0 to 15
	LRXA imm	3D20-3D3F*	·	·	·	2/3	X ←{ROM($\boxed{\text{imm}}\boxed{X}\boxed{Y}$)}d, d=7-4 AC←{ROM($\boxed{\text{imm}}\boxed{X}\boxed{Y}$)}d, d=3-0 imm=0 to 15
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	3D80-3D8F	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	·	·	↓Z	1/1	imm-(Y) ; imm=0 to 15

Table 5: INSTRUCTION SET SUMMARY (Continued)

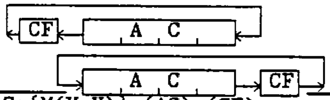
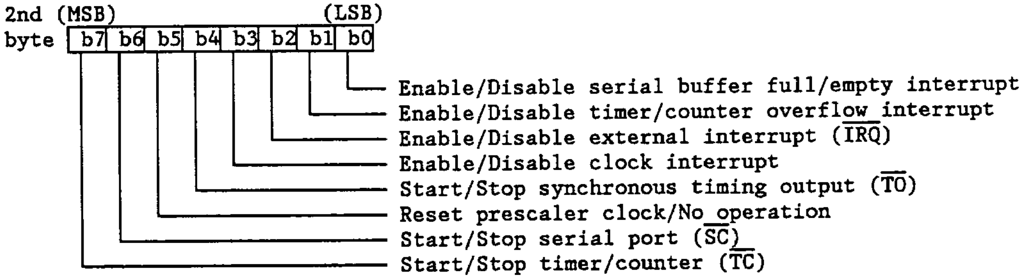
	Mnemonic +Operand	Code (Hex.)	Flag/Status			Byte/ Cycle	Operation
			ZF	CF	ST		
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruction)
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruction)
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1
	ICX	3DAC	·	·	↓C	2/2	X← (X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←$\overline{(AC)}$+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	·	·	·	2/2	System initialization
Input/ Output	ANDX	3DA8	·	·	·	2/2	E←(AC)∩(E)Y, Y=0 to 6
	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=8 to 12
	INK	12	↕	·	·	1/1	AC←(K)
	INX	3DAA	·	·	·	2/2	AC←(E)Y, Y=0 to 5
	ORX	3DA9	·	·	·	2/2	E←(AC)∪(E)Y, Y=0 to 5
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=8 to 11
	OUTO	01	·	·	·	1/1	O←(AC)
	OUTP	02	·	·	·	1/1	P←(AC)
	OUTX	03	·	·	·	2/2	(E)Y←AC, Y=0 to 5
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-6FFF*	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.

Table 5: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status			Byte/ Cycle	Operation
			ZF	CF	ST		
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00- 3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000- 7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{\text{IRQ}}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: MB88521, MB88522, and MB88523: AC←(SB), ZF affected
MB88525 : AC←(SBL), X←(SBH), ZF not affected

Symbols and Abreviations

Symbols	**Meaning**
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
-	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
(Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	**Meaning**
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
E	E-Port (#0: E3-E0, #1: E7-E4, ... ,#5: E23-E20)
IF	Interrupt flag
imm	Immediate data
$\overline{\text{IRQ}}$	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
O	O-Port (O3-O0)
P	P-Port (P3-P0)
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODES SUMMARY

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	* EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: ☐ : 1-byte/1-cycle instruction ◩ : 2-bytes/2-cycles instruction

* See the next page

Table 6: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DH \ 3DL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3	NOT USE															
4																
5																
6	NOT USE															
7																
8	AI imm	(ICA)														(DCA)
9	LXID imm															
A	SBA bp				RBA bp				ANDX	ORX	INX	OUTX	ICX	RST	NOT USE	
B	NOT USE															
C	NOT USE															
D																
E	NOT USE															
F																

Note: ◩ : 3 byte/3 cycle instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88520 series consists of the MB88521, MB88522, MB88523, and MB88525. The MB88528-101 and MB88528-102 are available as piggyback EPROM evaluation devices for MB88521 and MB88523. MB88528-301 and MB88528-302 is for MB88525. MB88PG522-102 is for MB88522.

Table 7: MB88520 SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88521-PSH MB88521-PF MB88523-PSH MB88523-PF	MB88522-PSH	MB88525-PSH	MB88528-CSH CSH-XXX	MB88PG528- -CSH-102
ROM Size	4K x 8 bits (MB88521) 2K x 8 bits (MB88523)	2K x 8 bits	4K x 8 bits	8K x 8 bits	
	(On-chip mak ROM)			(Piggyback EPROM)	
RAM Size (Directly addressed locations)	256 x 4 bits (0-7)				
I/O Port:	Total 57 lines				
-Input only port	4				
-Output only port	8				
-I/O port	30				
-Control port	5 (Including serial I/O)				
Output Port Type	· STD P/U · STD O/D · 12V-interface O/D (P-Port) (Mask option)			· 101/301: STD P/U · 102/302: O,R,E:Std O/D P: 12V-interface O/D	
Stack Depth (Nesting level)	8 levels				
Timer/Counter:	Yes				
-Buffer size	8 bits				
-Clock source	Internal/external				
Serial I/O:	Yes				
-Buffer size	4 bits		4/8 bits	4 bits (101/102) 4/8 bits (301/302)	4 bits
-Clock source	Internal/External				
-Output latch	Yes				
Clock Generator:	Yes				
-Oscillator type	· Crystal/External · RC-network/External (Mask option)			· Crystal/External (Fixed)	
-Clock Frequency (With prescaler)	0.5 MHz-3 MHz (1 MHz-6 MHz)				
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)			Yes (Fixed)	
Interrupt Function	Yes				
-Nesting level	Single level				
-Interrupt sources	4 sources				

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

Table 7: MB88520 SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS (Continued)

	MB88521-PSH MB88521-PF MB88523-PSH MB88523-PF	MB88522-PSH	MB88525-PSH	MB88528-CSH CSH-XXX	MB88PG528- -CSH-102
Standby Function:	Yes/No (Mask option)			Yes	No
-Initiation method	·Software			·Software	-
-Oscillator state during standby	·Idle/Stop (Sfotware selectable)			·Idle/Stop (Software selectable)	-
-Output state during standby	·Hold/High-Z (Mask option)			·Hold(102/103)/ High-Z(101/301)	-
-Standby Off Reset Function	·Yes/No (Mask option)			·No	-
Watch Dog Timer Function	Yes/no (Mask option)			No (Fixed)	
Number of Instructions	80			82	
Instruction Length/Cycle	1/1, 2/2, or 2/3			1/1, 2/2, 2/3, OR 3/3	
Min. Instruction Execution Time	2.0 µs at 6 MHz (With prescaler)				
Power Supply:	Single +5V				
-Active	· 4.5V to 5.5V				4.5Vto5.5V
-Standby	· 3.5V to 6.0V				-
Operating Temperature Range	-30°C to +70°C				
Process	CMOS				
Package	SH-DIP-64P FPT-64P	SH-DIP-64P		SH-MDIP-64C	
Development Tools:					
-Hardware	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Comomn) MB2115-37A : DUE board MB2115-04 : EPROM writer (Common)				
-Software	SM05215-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-A012: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-G022: PC-DOS host emulator				

Note: P/U: Pull-up
O/D: Open-drain
Std: Standard

ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM RATINGS†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Voltage	V_{OUT}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
		$V_{SS}-0.3$		$V_{SS}+15.0$	V	12V-interface open-drain
Output Low Current	I_{OL}			20	mA	
Total Output Low Current	ΣI_{OL}			80	mA	
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

• RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Guaranteed range
		3.5		6.0	V	Standby range
Input High Voltage	V_{IH}	$0.75 \cdot V_{CC}$		$V_{CC}+0.3$	V	E-, R-, K-Port, SI
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$, $\overline{SC}/\overline{TO}$
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.25 \cdot V_{CC}$	V	E-, R-, K-Port, SI
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	EX, START, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$, $\overline{SC}/\overline{TO}$
Operating Ambient Temperature	T_A	-30		+70	°C	

- **DC CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-,P-,R-,E-Ports (Standard pull-up) $\overline{\text{SC}}/\overline{\text{TO}}$, SO	V_{CC}=4.5V I_{OH}=-200µA	2.4			V
			V_{CC}=4.5V I_{OH}=-10µA	4.0			V
Output Low Voltage	V_{OL}	O-,P-,R-,E-Ports (All option) $\overline{\text{RESET}}$, $\overline{\text{SC}}/\overline{\text{TO}}$, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		O-,P-,R-,E-Ports (All option)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input leakage Current	I_{IL}	R-, E-Ports (Standard pull-up), $\overline{\text{SC}}/\overline{\text{TO}}$	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		EX, K-Ports, SI $\overline{\text{RESET}}$, $\overline{\text{TC}}$, $\overline{\text{IRQ}}$	V_{CC}=5.5V V_{IL}=0.4V			-60	µA
	I_{IH}	EX, START	V_{CC}=5.5V V_{IH}=5.5V			60	µA
Open-Drain Output Leakage Current	I_{LEAK}	P-Port (12V-interface open-drain)	V_{CC}=5.5V V_{OH}=13.2V			40	µA
		O-,P-,R-,E-Ports (Standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	µA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	O-,P-,R-,K-Ports (All option), $\overline{\text{IRQ}}$, $\overline{\text{SC}}/\overline{\text{TO}}$, SI, SO, $\overline{\text{TC}}$	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±10	µA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=1MHz(Operation) All outputs open		2	6	mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=6.0V(Max.) fc=0(Standby) All outputs open			15	µA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

2

- **AC CHARACTERISTICS**

CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/ Port	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock Frequency	f_C	EX, X	Crystal, ceramic or RC-network OSC. external clock drive Figs. 6, 7	0.5	3	MHz	Without prescaler
				1	6		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 6, 7	0.33	2	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive (with X open) Figs. 6, 7	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 6, 7	5	200	ns	

Fig. 6: CLOCK TIMING

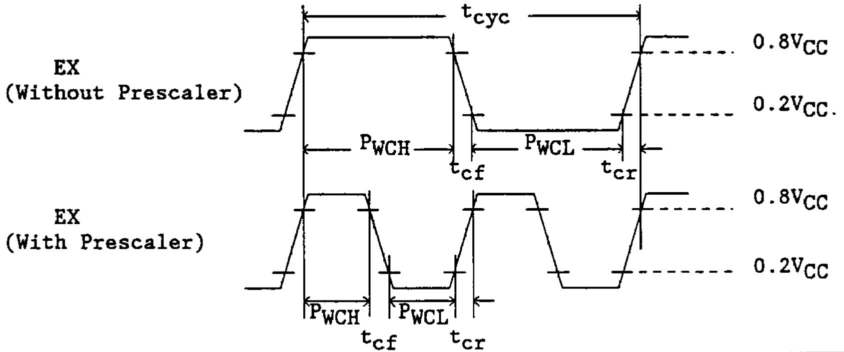
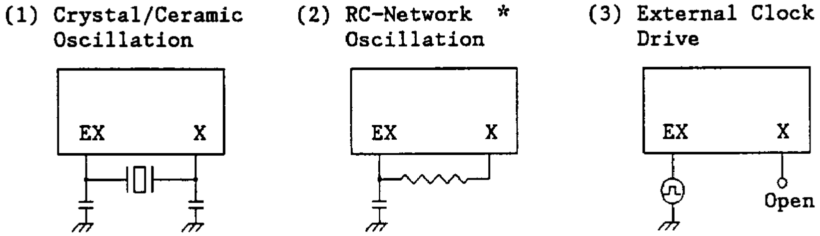


Fig. 7: CLOCK CIRCUIT CONFIGURATIONS

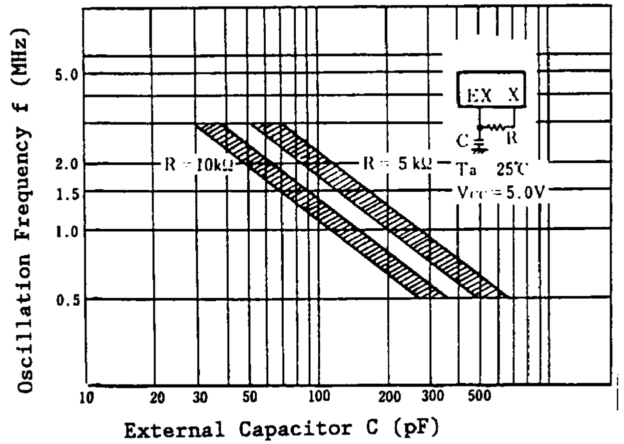

(1) Crystal/Ceramic Oscillation

(2) RC-Network * Oscillation

(3) External Clock Drive

* When the RC-network oscillation is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-30°C to +70°C
4) f_C does not exceed 3MHz (Max. setting clock frequency is about 2.4MHz at V_{CC}=5V and T_A=25°C.)

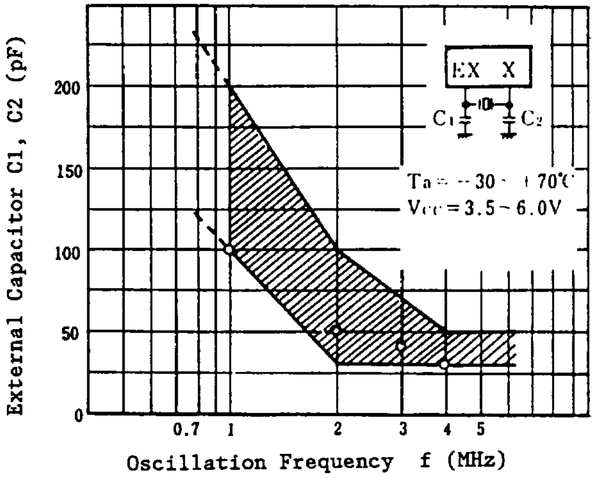
Fig. 8: RC-Network Oscillation Characteristics (Example)



Note:

When the RC-network oscillations is used, the following conditions must be met: 1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-30°C to 70°C 4) f_C does not exceed 2.4 MHz.

Fig. 9: Crystal Oscillation Characteristics (Example)



Note:

1) The cross-hatched portion shows an area where the on-chip oscillator has stable oscillation characteristics and short oscillation stabilization time when an average crystal resonator is used. This chart gives an aim value of the external capacitor to realize a desired oscillation frequency. When an exact oscillation frequency is needed, a capacitor value should be determined, adjusting to individual crystal resonator characteristics.
2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer oscillation stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend to use high-frequency crystal resonator with on-chip 1/2 prescaler.

- **OUTPUT TIMING** (Except MB88522)
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-ports Delay Time	t_{PDH}	O-port, P-port, R-port, E-port	Fig. 10		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 10		1000	ns
	T_{SDL}				350	

Note:
1. A 10kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 50pF + 1TTL. See figure below.

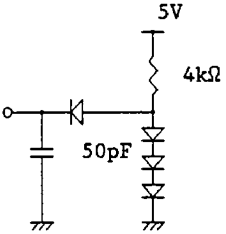
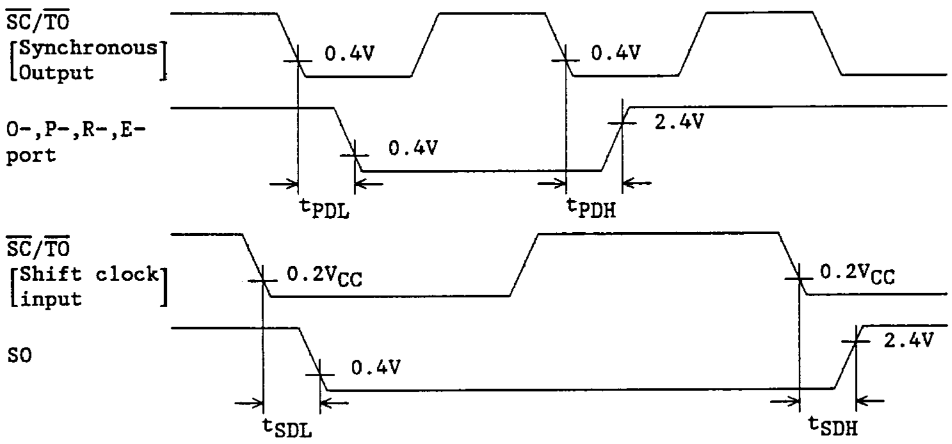


Fig. 10: OUTPUT CLOCK TIMING

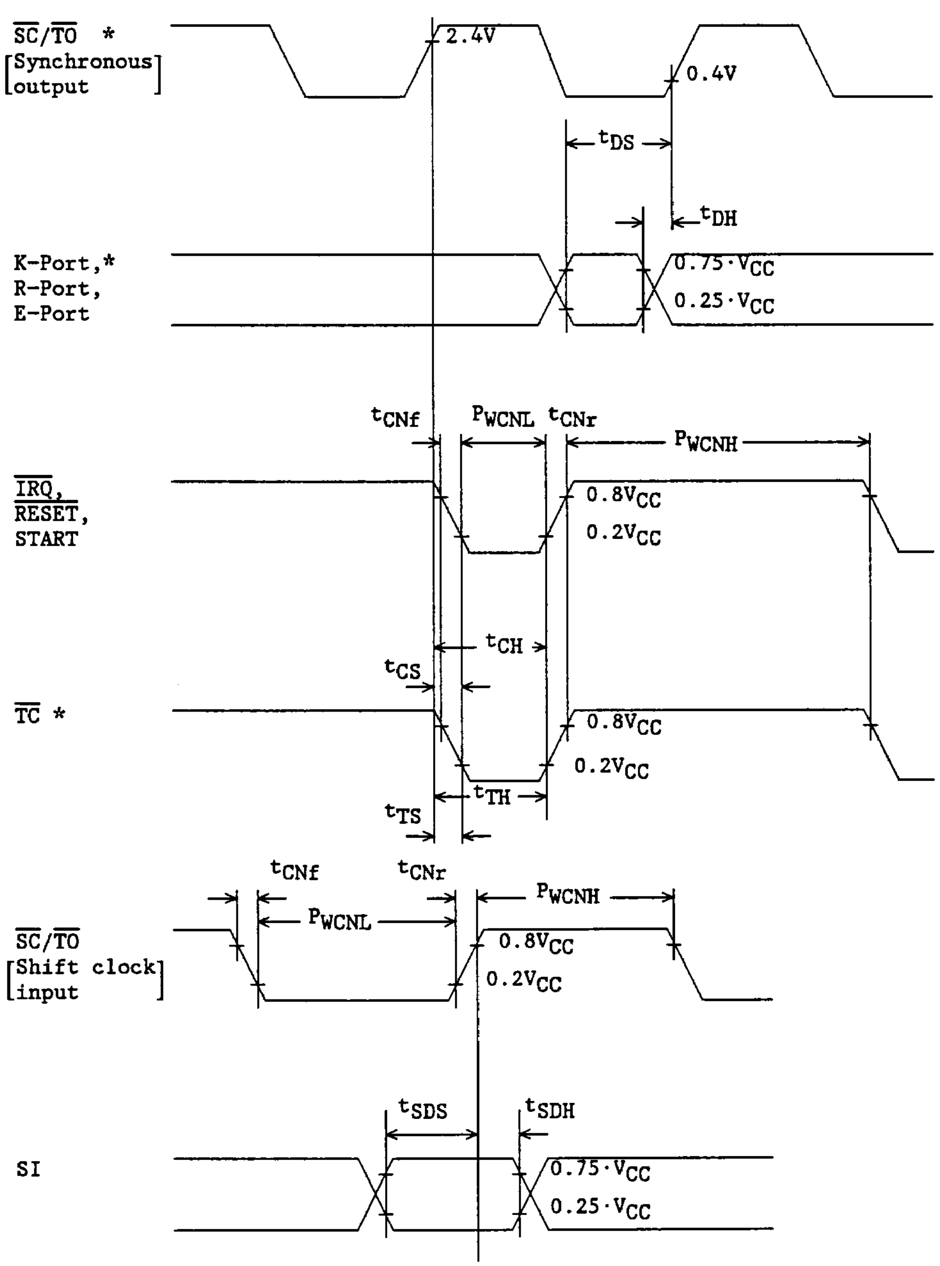


INPUT TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time *	t_{DS}	K-Port, R-Port, E-Port	Fig. 11	$t_{cyc}+1000$		ns
Input Data Hold Time *	t_{DH}				$t_{cyc}-50$	
SI Input Setup Time	t_{SDS}	SI	Fig. 11	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time * (Synchronous mode)	t_{CS}	$\overline{\text{RESET}}$	Fig. 11		$2t_{cyc}-200$	ns
		$\overline{\text{IRQ}}$			$2t_{cyc}-200$	
Device Control Hold Time * (Synchronous mode)	t_{CH}	$\overline{\text{RESET}}$	Fig. 11	$8t_{cyc}+50$		ns
		$\overline{\text{IRQ}}$		$2t_{cyc}+50$		
Timing Input Setup Time * (synchronous mode)	t_{TS}	$\overline{\text{TC}}$	Fig. 11		$2t_{cyc}-200$	ns
Timing Input Hold Time * (Synchronous mode)	t_{TH}	$\overline{\text{TC}}$	Fig. 11	$2t_{cyc}+50$		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{\text{SC}}/\overline{\text{TO}}$	Fig. 11	$6t_{cyc}+250$		ns
		$\overline{\text{IRQ}}$, $\overline{\text{TC}}$		$6t_{cyc}+250$		
		$\overline{\text{RESET}}$		$12t_{cyc}+250$		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{\text{SC}}/\overline{\text{TO}}$	Fig. 11	$12t_{cyc}+250$		ns
		$\overline{\text{RESET}}$, $\overline{\text{TC}}$, $\overline{\text{IRQ}}$		$6t_{cyc}+250$		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{\text{SC}}/\overline{\text{TO}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, $\overline{\text{TC}}$	Fig. 11	Should be less than 200ns		

* Except MB88522

Fig. 11: INPUT TIMING

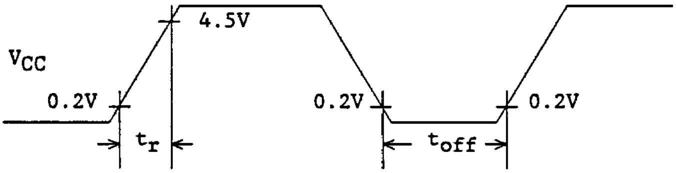


* Except MB88522

- **POWER-ON RESET**

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 12	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 12	1		ms	Required for accurate circuit operation repeatability

Fig. 12: POWER-ON RESET TIMING

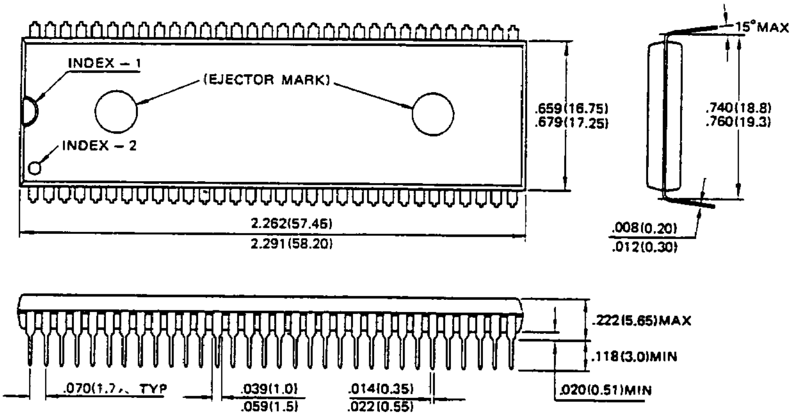


Note:
Power supply should be raised smoothly.

PACKAGE DIMENSIONS

- MB88521-PSH/MB88522-PSH/MB88523-PSH/MB88525-PSH: 64-PIN PLASTIC SHRINK DIP

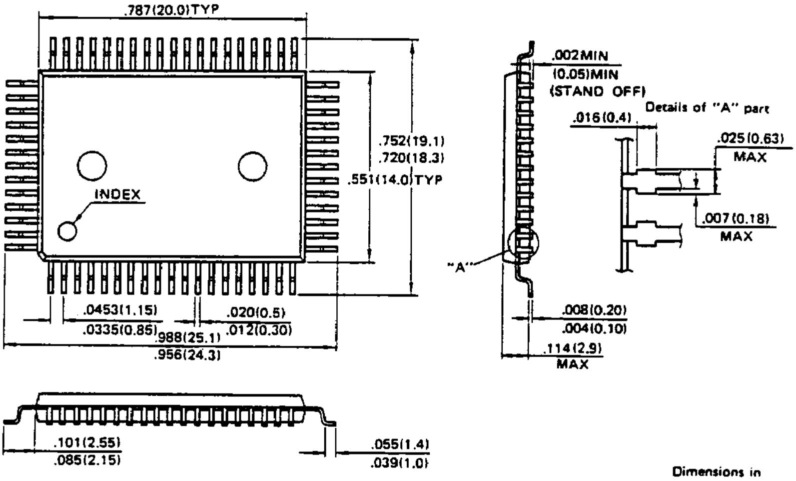
64-LEAD PLASTIC SHRINK DUAL IN-LINE PACKAGE
(CASE No.: DIP-64P-M01)



Dimensions in inches (millimeters)

- MB88521-PF/MB88523-PF: 64-PIN PLASTIC FLAT PACK

64-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-64P-M01)

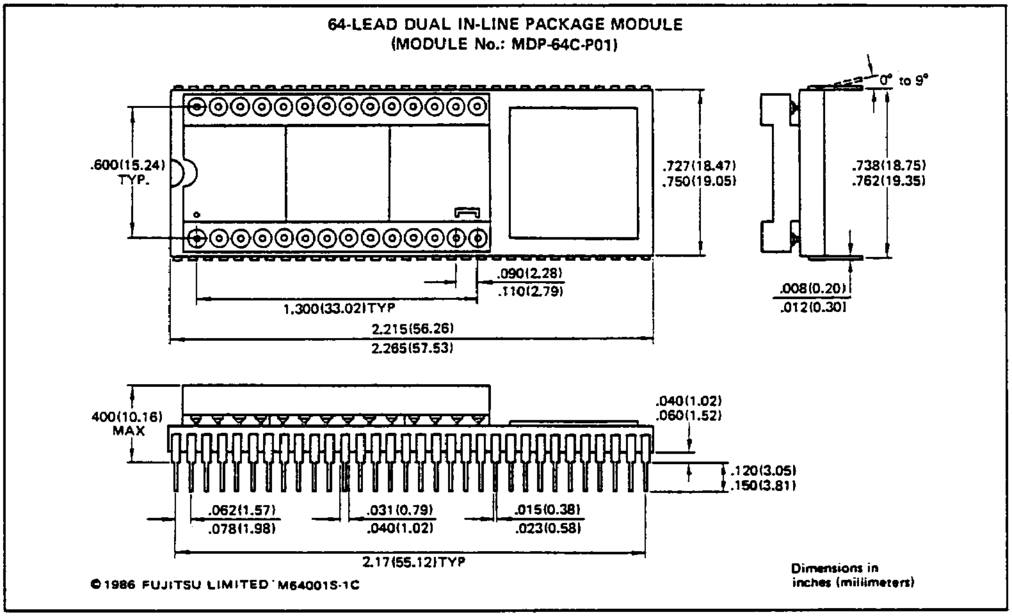


Dimensions in inchs (millimeters)

PACKAGE DIMENSIONS

- MB88528-CSH-101/-102/-301/-302
- MB88PG522-CSH-102

: 64-PIN CERAMIC SHRINK MDIP


64-LEAD DUAL IN-LINE PACKAGE MODULE
(MODULE No.: MDP-64C-P01)