FUJITSU

HIGH-PERFORMANCE CMOS SINGLE-CHIP 4-BIT MICRO-COMPUTER WITH ONE TIME PROM

MB88P551H
MB88P552H

TM333-B872: February 1987

ONE TIME PROGRAMMABLE READ ONLY MEMORY VERSION OF HIGH-SPEED CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER WITH MULTI I/O AND A/D CONVERTER

The Fujitsu MB88P551H and MB88P552H have One Time PROM (OTPROM) for program memory, they are include by the MB88550H series. Its architecture and instruction set are the same as the MB88551/551H and MB88552/552H, packaged in a same package.

MB88P551H contains a 8K by 8-bit OTPROM (program memory) whereas, the MB88P552H contains a 6K by 8-bit OTPROM. Besides the on-chip OTPROM, each devices has 256 by 4-bit static RAM (data memory), 68 I/O lines (including a serial I/O port with a 4-/8-bit buffer), an 8-bit timer/counter, a 5-bit resolution programmable successive approximation type A/D converter with 4 multiplex analog input, a 9-bit programmable pulse generator, and a clock generator.

Its instruction execution time is 1.5 μs to 12μs, MB88P551H/2H can cover the oscillation range of MB88550 and MB88550H series. These devices are fabricated by silicon-gate CMOS process, and packaged in an 80-pin plastic flat package (suffix -PF). It operate with +5V power supply over the temperature range of -30°C to +70°C.

For quickly provide, Fujitsu provide the two standard versions (-201 and -202). Also, Fujitsu can prepare the same option for MB88550 and MB88550H series, as a customer request.

For programming of the One Time PROM, Fujitsu provide the exclusive writer (MB2115-100 and -101) which include the MB2115 series. By use this writer, customer can write themselves. So customer can reduce the Turn Around Time, to change/modify the program is easy.

To minimize the system cost and development time. Fujitsu provides a complete complement of hardware and software development tools.

MB88P551H-PF/MB88P552H-PF
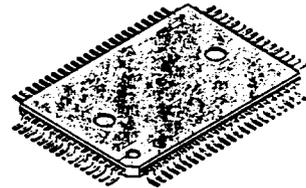
80-PIN PLASTIC FLAT PACKAGE (FPT-80P-M01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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FEATURES

- One Time PROM Version of CMOS Single Chip 4-bit Microcomputer

- Program Memory:
  o MB88P551H: 8K x 8-bit one time PROM
  o MB88P552H: 6K x 8-bit one time PROM

- Data Memory: 256 x 4-bit static RAM

- 68 I/O Lines:
  o R-Port: Four 4-bit parallel or 16 individual input/output
  o E-Port: Thirteen 4-bit parallel I/O or 52 individual output:
    Following E-Ports are assignment to another function.
    E24-E29: Serial I/O, interrupt input, timer/counter input, timing output,
             standby release input
    E30-E31: Pulse generator I/O
    E32-E35: Analog inputs

- Three Selectable Output Port (E-, R-Ports) Circuits, Every 4-bit Port with
  Mask Option:
  o Standard open-drain
  o Standard pullup (-201)
  o High-current open-drain (-202)

- 8-bit Programmable Timer/Counter with Auto-loading Function and Two Clock Modes:
  o Internal (Timer)
  o External (Counter)

- Software Selectable 4-/8-bit Serial Buffer with 3 Software Shift Clock Modes:
  o Internal clock
  o External clock
  o Software clock

- 5-bit Programmable A/D Converter with 4-multiplex Analog Inputs and Sample-
  hold Circuits (Successive approximation type converter)

- On-chip 9-bit Programmable Pulse Generator

- On-chip Clock Generator with 2 Mask Options:
  o External crystal/ceramic resonator or external clock drive (-201, -202)
  o External RC-network or external clock drive

- Selectable 1/2 Clock Prescaler for Expanding Clock Range with Mask Options:
  o Without prescaler (-201, -202)
  o With   prescaler

- Single Level Four Prior Source Maskable Interrupt:
  o External
  o Clock
  o Timer/counter overflow
  o Serial buffer full/empty

- 8-nesting Levels for Subroutine Call

FEATURES (Continued)

- Instruction Set : Same as the MB88550/550H series
  - Number of instructions : 82
  - Instruction length/cycle: 1, 2, or 3 byte(s)/1 , 2, or 3 cycle
  - Execution time   : 1.5 µs min. using 8 MHz clock with prescaler

- On-chip Power-on Reset Circuit

- Selectable Low Power Standby Function (Software initiation and hardware release) with Mask Option:
  - Yes
  - No (-201, -202)

- Two Selectable Output Port State During Standby with Mask Option:
  - Hold
  - High impedance

- Two Software Selectable Oscillation States During Standby:
  - Idle
  - Stop

- Selectable Standby Off Reset with Mask Option

- Two Selectable Output Port Level During Reset with Mask Option:
  - High level (-201, -202)
  - Low level

- Selectable Watch-dog Timer Function with Mask Option:
  - Yes
  - No (-201, -202)

- Power Dissipation:
  - 8 mA at fc=2 MHz typ. (Active mode) (-201, -202)
  - 1.5 mA at fc=0 MHz max. (Standby mode)

- +5V Power Supply (VCC):
  - 4.5V to 5.5V (Active mode)
  - 3.5V to 6.0V (Standby mode)

- Programming Power Supply (VPP):
  - 17.5V to 18.5V (Programming mode)
  - 4.5V to 5.5V   (Normal operation mode)

- Wide Operation Temperature Range: T_A= -30 °C to +70 °C

- Silicon Gate CMOS Technology

- 80-pin Plastic Flat Package: FPT-80P-M01

- To Programming, Exclusive Writer (MB2115-100, -101)

- Powerful Development Support (Refer to Table 8)

Note: -201 and -202 indicate the standard version suffix. (Ex. MB88P551H-PF-201)

Fig. 1: PIN ASSIGNMENT

MB88P551H/MB88P552H
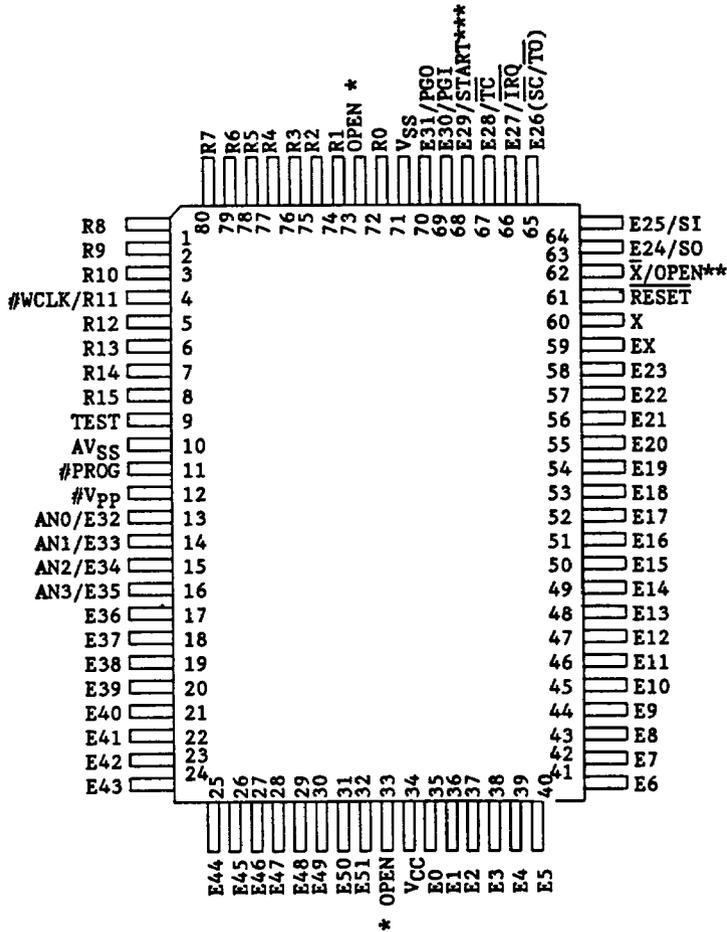
Note
  # These pins are used for the programming of internal OTPROM. (Pin assignment is different from MB88551/551H and MB88552/552H.
  * This pin should not to be connect.
 ** If selected oscillation output (-201, -202) by mask option, pin 62 is $\overline{X}$.
    If not, pin 62 is OPEN.
*** If selected standby by mask option, pin 68 is START pin. If not(-201, -202), pin 68 is E29 pin.
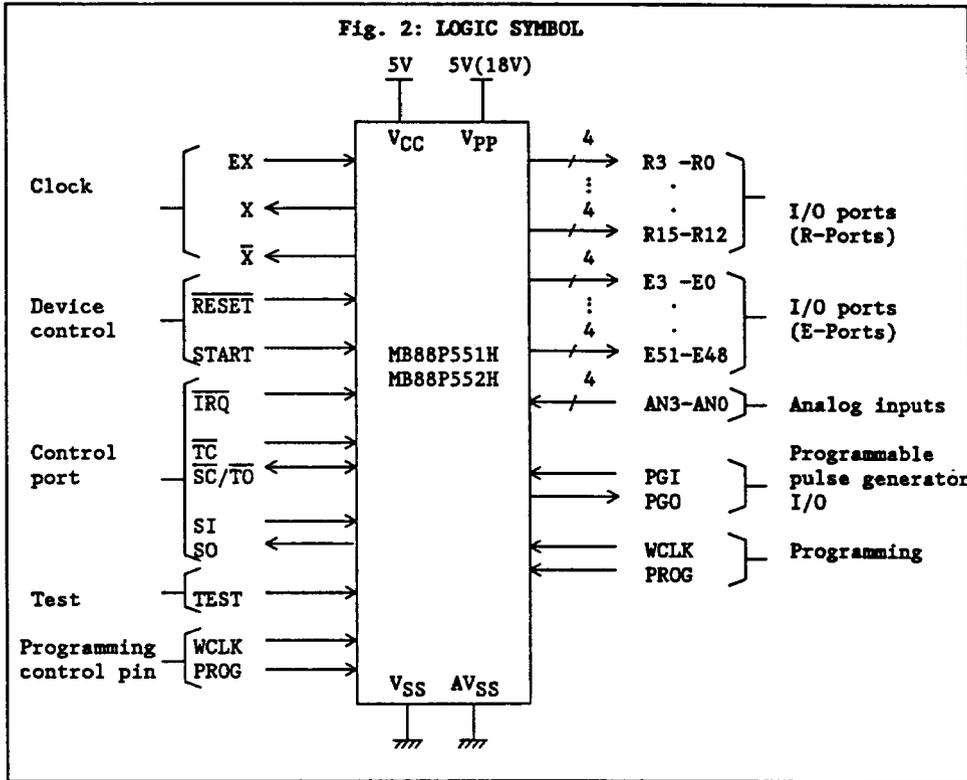
Fig. 2: LOGIC SYMBOL

Fig. 3: BLOCK DIAGRAM

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
RESET	61	I/O	This pin is a hysteresis input with an internal pullup resistor. An external capacitor from the RESET pin to the VSS pin (and the internal pull-up resistor), whose time constant should be greater than the reset time required (12 clock periods) composes the external reset circuit. Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the RESET pin, and then automatically returns high after it has passed 2^{18} clock periods since the oscillator starts by power on. This pin is a hysteresis input with an internal pullup resistor.
START	68	I	Start: A standby release input to the internal standby control and status registers that control and monitor the on-chip standby control circuit. A high level on the START pin during the standby mode sets the standby release flag (STF) in the standby status register, resets the standby enable flag (STBE) in the standby control register, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the VCC voltage must return to the active operation range (4.5V to 5.5V) when the battery backup is used. Also, the START pin must be low before the standby mode is initiated. The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the standby status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8). This pin is a hysteresis input with an internal pull-down resistor. If selected the E-Port by mask option, this pin is E29 pin. Standard devices (Suffix -201 and -202) are fixed at no standby function, so this pin assigned at E29 pin.

PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the
MB88P551H/552H.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	34	–	+5V DC power supply pin.
V_{SS}	71	–	Ground pin.
• Clock			
EX	59	I	Oscillator Input: Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ceramic oscillator is selected, and a hysteresis input when the RC-network oscillation is selected. Standard version devices (Suffix -201 and -202) are fixed at crystal/ceramic resonator.
X	60	O	Oscillator Output: Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation methods can be selected using mask option. When an external oscillator is used, the X pin should be left open.
$\overline{X}$	62	O	Clock Output: If selected oscillation output by mask-option, this pin output the inverting clock for external sync functions. Standard version devices (Suffix -201 and -202) are fixed at clock output.
• Device Control			
$\overline{RESET}$	61	I/O	Reset: This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{RESET}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port			
$\overline{\text{IRQ}}$	66	I	**Interrupt Request:** A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{\text{IRQ}}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register re-gardless of enabling or disabling the external inter-rupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{\text{IRQ}}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{\text{IRQ}}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pullup resistor, and common to E27 pin.
$\overline{\text{TC}}$	10	I	**Timer/Counter:** An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{\text{TC}}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B). Also, the $\overline{\text{TC}}$ pin state (logical level), which is reflected in the timer/counter input flag (TCF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (count-er) mode, is testable by reading the prescaler select register using IN instruction (with Y = B). (When $\overline{\text{TC}}$ = L, TCF = 1; otherwise TCF = 0.) This pin is inactive as a count clock input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pullup resistor.
$\overline{\text{SC}}/\overline{\text{TO}}$	65	I/O	**Shift Clock/Timing Output:** One of the shift clock input ($\overline{\text{SC}}$), shift clock output ($\overline{\text{SC}}$), or synchronous timing output ($\overline{\text{TO}}$) is enabled using EN instruction.
		I	$\overline{\text{SC}}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{\text{SC}}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the exter-nal clock mode is not selected or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input.

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Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
$\overline{SC}/\overline{TO}$	65	I/O	2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization. $\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. This $\overline{SC}/\overline{TO}$ pin is common to E26 pin.
SI	64	I	Serial Data Input: Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shift clock shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instruction (with Y = A). This pin is a non-hysteresis input with an internal pullup resistor and common to E25 pin.
SO	63	O	Serial Data Output: Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appears on the SO pin. This pin is a CMOS pull up output, and is set high by reset. This pin is common to E24 pin.
PGI	69	I	Programmable Pulse Generation Start Input: Programmable pulse generation started by TADT instruction, 9-bit pulse generation timer counted by rising or falling of PGI pin. This pin is common to E30 pin.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
PGO	70	O	**Programmable Pulse Generator Output:** When 9-bit pulse generation timer is overflow, first PGO pin output is fall. And secondly overflow, PGO pin output is rise. This pin is common to E31 pin.
• I/O Ports			
R3 –R0, R7 –R4, R11-R8, R15-R12	76-74,72 80-77, 4- 1, 8- 5,	I/O	**R-Port:** This port functions as four 4-bit parallel input (non-latched)/output (latched) port, or 16 individual input (non-latched)/output (latched) lines, depending on instructions. Parallel I/O: Each port is named as R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R15-R12), and indirectly addressed by the Y-register. A 4-bit data on an addressed port is input into the accumulator by IN instruction. (Before IN instruction, the addressed port must be setup to "1" (input mode).) And further the R-Port #3 is directly input into accumulator by INK instruction. A 4-bit data in the accumulator is output onto an addressed port of R-Port #0 to #3 by OUT instruction. Individual I/O: Each line of R15 to R0 is indirectly addressed by the Y-register, and addressed line is individually set/reset by SETR/RSTR instruction, and further each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. All lines are testable using TSTR instruction, and further each line of R-Port #2 (R11-R8) is directly testable by TSTD instruction. (Before TSTR and TSTD instructions, the addressed line must be setup to "1" (input mode).) Refer to Table 4 User mask options for available making option. R11 pin is common to WCLK pin. For standard version devices, port option of suffix -201 is standard pullup, suffix -202 is standard open-drain output.
E3 –E0, E7 –E4, E11-E8, E15-E12, E19-E16, E23-E20, E27-E24, E31-E28, E35-E32, E39-E36, E43-E40, E47-E44, E51-E48	38-35, 42-39, 46-43, 50-47, 54-51, 58-55, 66-63, 70-67, 16-13, 20-17, 24-21, 28-25, 32-29	I/O	**E-Ports:** This functions as thirteen 4-bit parallel input (non-latched)/output (latched) port, or 52 individual output (latched) lines. Parallel I/O: Each port is named as E-Port #0 (E3-E0), E-Port #1 (E7-E4) ... E-Port #C (E51-E48), and indirectly addressed by Y-resister. A 4-bit data on an addressed port is input into the accumulator by INX (before INX instruction, the addressed port must be setup to "1" (input mode).)instruction. A 4-bit data in the accumulator is output onto an addressed port of E-Port #0 to #C by OUTX instruction and further in the E-Port #0 (E3-E0) and E-Port #1 (E7-E4) 4-bit data in

Symbol	Pin No.	Type	Name & Function
• I/O Ports (Continued)			
E3 -E0, E7 -E4, E11-E8, E15-E12, E19-E16, E23-E20, E27-E24, E31-E28, E35-E32, E39-E36, E43-E40, E47-E44, E51-E48	38-35, 42-39, 46-43, 50-47, 54-51, 58-55, 66-63, 70-67, 16-13, 20-17, 24-21, 28-25, 32-29	I/O	the accumulator is directly output onto the E-Port #0, and E-Port #1 by OUTP, OUT0 instruction. Individual output: Each line of E51 to E0 can be individually outputs by combined of ANDX, ORX, and OUTX instruction. Refer to Table 4 User mask options for available making option. E24 to E31 and E32 to E35 pin are common to control port and A/D converter pin. For standard version devices, port option of suffix -201 is standard pullup, suffix -202 is standard open-drain output.
TEST	9	I	Test Pin: Used to activate the test.mode for the shipping test purpose only at Fujitsu. This pin is normally set to a High logic level with an internal pullup.
OPEN	73,33	-	Open: This pin should not to be connect.
• A/D Converter			
AV$_{SS}$	10	-	A/D converter ground pin.
AN3-AN0	16-13	I	5-bit Resolution A/D Converter Input: There are four programmable approximation 5 bits resolution A/D conversion, the analog input port is selected with the analog input select register (Y=D). The A/D converter is activate by writing 1 to bit 0 of the control register (Y=9). Upon completion of A/D conversion results go into the A/D data register (high-order) (Y=F); the last two bits go into the A/D data register (low-order) (Y=E). This analog input is common to E35 to E32. In standby mode, this function doesn't worked, and A/D converted data is not hold.
• Programming			
VPP	12	-	PROM supply pin: +18V/+5V power supply pin. When program to the internal PROM, +18V power supply connect to this pin. In normal operation (non-programming mode), should be connect to the VCC pin for internal PROM.
PROG	11	I	Programming: Program enable signal input for data program to the internal PROM. When data program to the internal PROM, set to a High for enable the programming. In operation, set to a Low for disable the programming.
WCLK	4	I	Programming Clock: Programming pulse input for data program to the internal PROM. When data program to the internal PROM. This pin is common to R11 pin.

DIFFERENCES BETWEEN MB88550/550H SERIES AND MB88P551H/P552H

Following differences are user requested option (customized) devices (MB88P551H/552H-5XX) and MB88551/2, MB88551H/2H. User requested option is indicate by suffix as -5XX.

Table 2: DIFFERENCES BETWEEN MB88P550/550H SERIES AND MB88P551H/552H

Device\Item	MB88551/2	MB88551H/2H	MB88P551H/2H	Notes
ROM	Internal mask ROM	Internal mask ROM	Internal One Time PROM	
Pin: – Pin 4	· R11	· R11	· R11/WCLK	Common pin
– Pin 9	· Open	· Open	· TEST	This pin can open as a Open pin.
– Pin 11	· AVR–	· AVR–	· PROG	MB88P551H/2H have a no AVR– pin. So, AVR– set to GND automatically.
– Pin 12	· AVCC	· AVCC	· VPP	MB88P551H/2H have a no AVCC pin. So, AVCC set to VCC automatically.
fc (Clock frequency*)	Min. 0.5MHz	Min. 2 MHz	Min. 0.5MHz	MB88P551H/2H can cover mask ROM parts' H and non-H.
	Max. 3 MHz	Max. 4 MHz	Max. 4 MHz	
Min. instruction cycle	2.0 µs	1.5 µs	1.5 µs	

ICC
(VCC active
  supply
  current)
	ICC=3mA (Typ)
	(fc= 1MHz,
	VCC=5.0V,
	Outputs open)
		ICC=5mA (Typ)
		(fc= 2MHz,
		VCC=5.0V,
		Outputs open)
			ICC=8mA (Typ)
			(fc= 2MHz,
			VCC=5.0V,
			Outputs open)	

IA
(AVCC active
  supply
  current)
	IA=3mA (Typ)
	(fc= 1MHz,
	VCC=5.0V,
	Outputs open)
		IA=3mA (Typ)
		(fc= 2MHz,
		VCC=5.0V,
		Outputs open)
			–	IA is include in a ICC

IPP (VPP normal operation supply current)	–	–	IPP=1mA (Typ) (fc= 1MHz, VCC=VPP=5.0V, Outputs open)	Normal Operation mode only.

* Without prescaler

Table 2: DIFFERENCES BETWEEN MB88P550/550H SERIES AND MB88P551H/552H (Continued)

Device / Item	MB88551/2	MB88551H/2H	MB88P551H/2H	Notes
IPP (VPP Programming supply current)	–	–	IPP=30mA (Max) (fc= 1MHz, fWCLK=20Hz, VCC=5.5V, VPP=18.0V, Outputs open)	Programming mode only
ICCH (VCC standby supply current)	Max. 15μA (fc=0Hz, VCC=6.0V, Outputs open)	Max. 15μA (fc=0Hz, VCC=6.0V, Outputs open)	Max. 1.5mA (fc=0Hz, VCC=6.0V, Outputs open)	In standby, MB88P551H/2H flow the current through A/D bias resistor.
IAH (AVCC standby supply current)	Max. 5μA (fc=0Hz, AVCC=5.5V, Outputs open)	Max. 5μA (fc=0Hz, AVCC=5.5V, Outputs open)	–	
IPPH (VPP standby supply current)	–	–	Max. 10μA (fc=0MHz, Vcc=Vpp=6.0V Outputs open)	
Output Port Level During Reset	Except R12–R15 can select Low level by mask option.	Except R12–R15 can select Low level by mask option	Except R0–R7 and R12–R15 can select Low level by mask option.	

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pullup, and all output-only and input/output pins except E- and R-Ports have push-pull output buffer (standard pullup). E- and R-Ports can have push-pull (standard pullup) or open-drain (standard or high-current) buffer using mask option.

Table 3: INPUT/OUTPUT CIRCUIT

Pin	Circuit	Remarks
EX X $\overline{\text{X}}$	• Crystal/Ceramic OSC or external clock* (201, 202)	1. Non-hysteresis inverter 2. Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V) * When only external clock drive is used, we recommend RC-network OSC. Oscillation output option a: Yes (201, 202) b: No
EX X $\overline{\text{X}}$	• RC-network OSC or external clock*	1. Hysteresis inverter 2. Without feedback resistor * When only external clock drive is used, we recommend RC-network OSC. Oscillation output option a: Yes (201, 202) b: No
$\overline{\text{RESET}}$		• Hysteresis inverter • With output pullup resistor (P-ch. Tr.): approx. 300kΩ
R0-R10, R12-R15, E0-E23, E36-E51		• Output port option 1: Standard pullup (201): pullup resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain(202): Without P-ch. pullup resistor

Input/Output Circuit (Continued)

Pin	Circuit	Remarks

E24/SO
 	
E31/PG0
		• Output port option
		  1: Standard pullup(201):
		     pullup resistor:
		     P-ch. Tr. approx. 10kΩ
		  *2: Standard/high-current
		     open-drain(202):without
		     P-ch. pullup resistor

E25/SI
E27/$\overline{IRQ}$
E28/$\overline{TC}$
E30/PGI
		• Output port option
		  1: Standard pullup:
		     pullup resistor(201):
		     P-ch. Tr. approx. 10kΩ
		  *2: Standard/high-current
		     open-drain(202):without
		     P-ch. pullup resistor
		
		**$\overline{IRQ}$, $\overline{TC}$: Hysteresis
		            inverter

E26($\overline{SC}$/$\overline{TO}$)		• Output port option
		  1: Standard pullup(201):
		     pullup resistor:
		     P-ch. Tr. approx. 10kΩ
		  *2: Standard/high-current
		     open-drain(202):without
		     P-ch. pullup resistor
		
		** A circuit is added to
		temporarily turn on the
		transistor connected to the
		power supply and to immedi-
		atly, raise the pin to the
		high level by the timing H
		output to the pin.

E29/START		E29:
		• Output port option
		  1: Standard pullup(201):
		     pullup resistor:
		     P-ch. Tr. approx. 10kΩ
		  2: Standard/high-current
		     open-drain(202):without
		     P-ch. pullup resistor
		START:
		  With N-ch. pull-down
		  resistor approx. 300kΩ

Input/Output Circuit (Continued)

Pin	Circuit	Remarks
E32/AN0 to E35/AN3	Analog input	• Open-drain output
PROG		• Input pull-down resistor approx. 100kΩ (At Vcc=5V)
R11/WCLK	* Write clock	• Output port option 1: Standard pullup (201): pullup resistor: P-ch. Tr. approx. 10kΩ *2: Standard/high-current open-drain(202): Without P-ch. pullup resistor
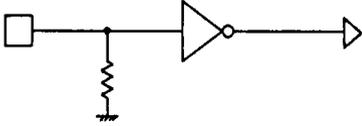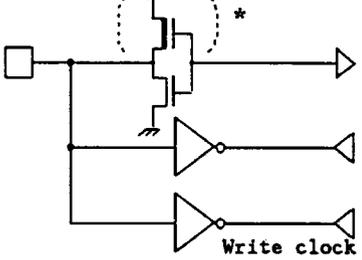
3

USER MASK OPTIONS

The MB88P551H/P552H-5XX which user requested option version has the following mask options. (Standard version is refer Table 5 STANDARD VERSION OPTIONS)

Table 4: MB88550H SERIES CUSTOMIZED USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock Prescaler	CLK	No	0	f_C=0.5 MHz to 1 MHz
		Yes	1	f_C=1 MHz to 8 MHz
Oscillation Circuit	OSC	Crystal/Ceramic OSC or external clock	0	When only external clock drive is use, we recommend RC-network oscillator. (201,202)
		RC-network OSC	1	Recommend a without clock prescaler.
Oscillation Output	CLO	No	0	
		Yes	1	(201,202)
Port Scramble		No	0	(201,202)
		Yes	1	Port scramble is appointed every 4-bit.
Output Port (R-, E-Port) Type	PORT	High-current open-drain	1/K	(202)
		Standard open-drain	2/L	(201)
		Standard pull-up	3/M	Except E35 to E32 E26 pin is fix
Standby Function	STRT	No	0	Pin 68 used as E29 (201,202)
		Yes	1	Pin 68 used as START
Output Port State During Standby	STATE	Hold	0	
		High-Z	1	
Standby off Reset Function	SOR	No	0	
		Yes	1	
Watch Dog Timer	WDR	No	0	(201,202)
		Yes	1	
Output Port Level During Reset	RST	High level	0	(201,202)
		Low level	1	Except R0-R15

Table 4: USER MASK OPTIONS (Continued)

When port scramble selected, output port circuit option table.

PIN NO.	PIN NAME	OUTPUT PORT OPTION	OUTPUT PORT DURING RESET
1 to 4	R8 to R11	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL
5 to 8	R12 to R15	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL
13 to 16	E32/AN0 to E35/AN3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN	☐ HIGH LEVEL ☐ LOW LEVEL
17 to 20	E36 to E39	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
21 to 24	E40 to E43	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
25 to 28	E44 to E47	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
29 to 32	E48 to E51	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
35 to 38	E0 to E3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
39 to 42	E4 to E7	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
43 to 46	E8 to E11	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
47 to 50	E12 to E15	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
51 to 54	E16 to E19	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
55 to 58	E20 to E23	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
63 to 66	E24/SO to E27/$\overline{\text{IRQ}}$	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN *5 ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL
67 to 70	E28/$\overline{\text{TC}}$ to E31/PG0	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN *6 ☐ STANDARD PULL-UP	☐ HIGH LEVEL ☐ LOW LEVEL *6
72, 74 75, 76	R0 to R3	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL
77 to 80	R4 to R7	☐ HIGH CURRENT OPEN-DRAIN ☐ STANDARD OPEN-DRAIN ☐ STANDARD PULL-UP	☐ HIGH LEVEL

*5 Output port of E26($\overline{\text{SC}}$/$\overline{\text{TO}}$) is applied to only standard pull-up.
*6 When the standby function is selected, E29/START is input port.

Fujitsu prepared two standard option (Suffix -201 or -202) for MB88P551H/2H and they have the following mask options. For unselected options, Fujitsu can supply for suffix -5XX (Refer to Table 4)

Table 5: MB88P551H/552H -201 AND -202 STANDARD VERSION MASK OPTIONS

Optional Feature	Symbol	MB88P551H-201 MB88P552H-201	MB88P551H-202 MB88P552H-202	Note
Clock Prescaler	CLK	Yes	Yes	fc=1MHz to 8MHz
Oscillator Output	CLO	Yes	Yes	
Oscillator Type	OSC	Crystal/ceramic OSC or external clock*	Crystal/ceramic OSC or external clock*	
Port Scramble		No	No	
Output Port Type	PORT	Standard pull-up	High-current open-drain	
Standby Function	STRT	No	No	
Output Port State During Standby	STATE	-	-	
Standby Off Reset Function	SOR	-	-	
Watch-dog Timer Function	WDR	No	No	
Output Port Level During Reset	RST	High	High	

NOTES ON OPERATION

• **Latch-up Prevention**

Latch-up may occur in CMOS devices following treatments:

(1) The voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pin.
(2) The voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins.
(3) MCU power supply (V_{CC}) power-on after analog power supply (AV_{CC}) power-on.

If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

• **Treatment of Unused Pins**

Unused input pins should be externally pulled up or down with resistors because such unused input pins may cause some malfunction if they are left open. (However, the X pin should be open when an external clock oscillator is used.)

• **External Capacitors for Crystal Oscillation**

Fig. 7 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

• **Supply Voltage**

Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:

(1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
(2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

• These devices are different from production version devices, so, note that Table 2 DIFFERENCES BETWEEN MB88P550/550H SERIES AND MB88P551H/552H.

INSTRUCTION SET DESCRIPTION

The MB88P551H and MB88P552H instruction set includes 82 instructions, 78% of which are single-byte and single-cycle, 18% two-byte two-cycles, 1% two bytes three-cycles, and 2% three-bytes and three-cycles. The MB88P551H and MB88P552H instruction set are same as the MB88550/550H series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 6 and 7 summarize the MB88P551H and MB88P552H instruction set.

Table 6: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	ZF	CF	ST	Byte/ Cycle	Operation
Register- to- Register Transfer	TATC	05	•	•	•	1/1	$TH \leftarrow (X)$, $TL \leftarrow (AC)$
	TADT	06	•	•	•	1/1	$DT_9 \leftarrow (CF)$, $DT_{8-4} \leftarrow (X)$, $DT_{3-0} \leftarrow (AC)$
	TAS	07	•	•	•	1/1	$SB \leftarrow (AC)$
	TAY	04	•	•	•	1/1	$Y \leftarrow (AC)$
	TSA	17	•	•	•	1/1	4-bit mode: $AC \leftarrow (SB_L)$, 8-bit mode: $AC \leftarrow (SB_L)$, $X \leftarrow (SB_H)$
	TTCA	15	•	•	•	1/1	$X \leftarrow (TH)$, $AC \leftarrow (TL)$
	TAPW	16	•	•	•	1/1	$PW_9 \leftarrow (CF)$, $PW_{8-4} \leftarrow (X)$, $PW_{3-0} \leftarrow (AC)$
	TYA	14	$\updownarrow$	•	•	1/1	$AC \leftarrow (Y)$
	XX	1B	$\updownarrow$*1	•	•	1/1	$(AC) \rightleftharpoons (X)$
Register- to- Memory Transfer	L	0D	$\updownarrow$	•	•	1/1	$AC \leftarrow \{M(X,Y)\}$
	LS	2B	$\updownarrow$	•	•	1/1	$SB \leftarrow \{M(X,Y)\}$
	ST	1D	•	•	•	1/1	$M(X,Y) \leftarrow (AC)$
	STDC	1A	•	•	$\downarrow$C	1/1	$M(X,Y) \leftarrow (AC)$, $Y \leftarrow (Y)-1$
	STIC	0A	•	•	$\downarrow$C	1/1	$M(X,Y) \leftarrow (AC)$, $Y \leftarrow (Y)+1$
	STS	2A	$\updownarrow$	•	•	1/1	$M(X,Y) \leftarrow (SB)$
	X	0B	$\updownarrow$*1	•	•	1/1	$(AC) \rightleftharpoons \{M(X,Y)\}$
	XD D	50-53*	$\updownarrow$*1	•	•	1/1	$(AC) \rightleftharpoons \{M(0,D)\}$; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	$\updownarrow$*2	•	•	1/1	$(Y) \rightleftharpoons \{M(0,D)\}$; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	$\downarrow$	•	•	1/1	$AC \leftarrow 0$ (Included in LI instruction)
	LI imm	90-9F*	$\updownarrow$	•	•	1/1	$AC \leftarrow imm$; imm=0 to 15
	LXI imm	58-5F*	$\updownarrow$	•	•	1/1	$X3 \leftarrow 0$, X2 to X0$\leftarrow imm$; imm=0 to 7
	LXID	3D90- 3D9F*	$\updownarrow$	•	•	2/2	$X \leftarrow imm$; imm=0 to 15
	LRXA imm	3D20- 3D3F*	•	•	•	2/3	$X \leftarrow \{ROM(\boxed{\text{imm} \mid X \mid Y})\}d$, d=7-4 $AC \leftarrow \{ROM(\boxed{\text{imm} \mid X \mid Y})\}d$, d=3-0 imm=0 to 31
	LYI imm	80-8F*	$\updownarrow$	•	•	1/1	$Y \leftarrow imm$; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	$\updownarrow$	$\updownarrow$	$\downarrow$C	1/1	$AC \leftarrow (AC)+\{M(X,Y)\}+(CF)$
	AI imm	3D80- 3D8F	$\updownarrow$	$\updownarrow$	$\downarrow$C	1/1	$AC \leftarrow (AC)+imm$; imm=0 to 15
	AND	0F	$\updownarrow$	•	$\downarrow$Z	1/1	$AC \leftarrow (AC) \cap \{M(X,Y)\}$
	C	2E	$\updownarrow$	$\updownarrow$	$\downarrow$Z	1/1	$\{M(X,Y)\}-(AC)$
	CI imm	B0-BF*	$\updownarrow$	$\updownarrow$	$\downarrow$Z	1/1	$imm-(AC)$; imm=0 to 15
	CYI imm	A0-AF*	•	•	$\downarrow$Z	1/1	$imm-(Y)$; imm=0 to 15

Table 6: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICX	3DAC	·	·	↓C	2/2	X←(X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	[CF]←[A , C]←
	ROR	1C	↕	↕	↓C	1/1	→[A , C]→[CF]
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipula- tion	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00- 3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00- 3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	·	·	·	2/2	System initialization
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=8 to 12, 14, 15
	INK	12	↕	·	·	1/1	AC←(K)
	INX	3DAA	·	·	·	2/2	AC←E(Y) ; Y=0 to 12
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=8 to 11, 13
	OUTO	01	·	·	·	1/1	E3-E0←(AC)
	OUTP	02	·	·	·	1/1	E8-E4←(AC)
	OUTX	3DAB	·	·	·	2/2	(E)Y←AC; Y=0 to 12
	ANDX	3DA8	·	·	·	2/2	E←(AC)∩{(E)Y}; Y=0 to 12
	ORX	3DA9	·	·	·	2/2	E←(AC)∪{(E)Y}; Y=0 to 12
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000- 6FFF*	·	·	·	2/2	If ST=1, Subroutine call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.
	CALX addr	3D4000- 3D5FFF*	·	·	·	3/3	If ST=1, Subroutine call for addr; addr=0 to 8191. *4 ST=0, Not subroutine call.

Table 6: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status			Byte/ Cycle	Operation
			ZF	CF	ST		
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00-3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000-7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No branch.
	JPLX addr	3DC000--3DDFFF*	·	·	·	3/3	If ST=1, Branch to addr; addr=0 to 8191. *4 ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return from interrupt routine
	RTS	2C	·	·	·	1/1	Return from subroutine
Flag Manipula-tion	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:

2nd (MSB)   (LSB)
byte [b7 b6 b5 b4 b3 b2 b1 b0]

— Enable/Disable serial buffer full/empty interrupt
— Enable/Disable timer/counter overflow interrupt
— Enable/Disable external interrupt ($\overline{IRQ}$)
— Enable/Disable clock interrupt
— Start/Stop synchronous timing output ($\overline{TO}$)
— Reset prescaler clock/No operation
— Start/Stop serial port ($\overline{SC}$)
— Start/Stop timer/counter ($\overline{TC}$)
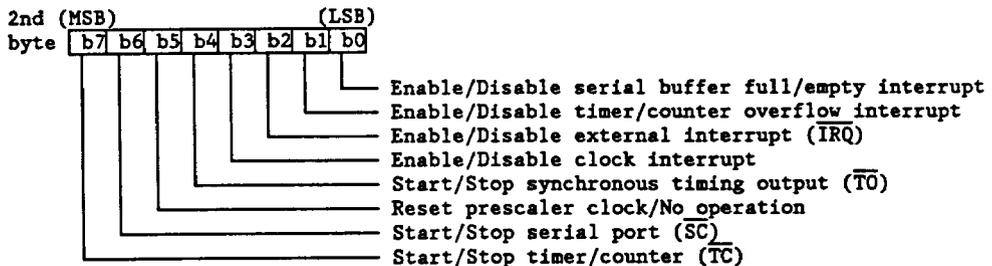
*4: addr=6144 to 8191 for MB88P551H only

MB88P551H   FUJITSU
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Table 7: INSTRUCTION CODES SUMMARY

H \ L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	OUTP	OUT	TAY	TATC	TADT	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTCA	TAPW	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	EXT *	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: ☐ : 1-byte/1-cycle instruction   ◹ : 2-bytes/2-cycles instruction

* See the next page   3-63

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
(Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
DT	Program delay timer for programmable pulse generator
E	E-Port (#0: E3-E0, #1: E7-E4,... #B: E47-E43, #C: E51-E48)
(E)Y; Y=n	E-Port #n specified by Y-register (E=0 to C)
IF	Interrupt flag
imm	Immediate data
IRQ	Interrupt request
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
PW	Pulse width latch for programmable pulse generator
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SBH	Serial buffer high register
SBL	Serial buffer low register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

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Table 7: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DL / 3DH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0								JPXY addr		MB88P551H only						
1																
2								LRXA imm		MB88P551H only						
3																
4								CALX addr		MB88P551H only						
5																
6								Not Used								
7																
8		(ICA)						AI imm								(DCA)
9								LXID imm								
A	SBA				RBA				ANDX	ORX	INX	OUTX	ICX	RST	Not Used	
B								Not Used								
C								JPLX		MB88P551H only						
D																
E								Not Used								
F																

Note: ☐ : 3 bytes/3 cycles instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88P551H/552H consists of the standard version (MB88P551H/552H-PF-201 and MB88P551H/552H-PF-102) and customized devices (MB88P551H/552H-5XX).

Table 8: MB88P505H PRODUCT LINE-UP & DEVELOPMENT TOOLS

Devices　　　Contents	MB88P551H -PF-201	MB88P552H -PF-201	MB88P551H -PF-202	MB88P552H -PF-202	MB88P551H -PF-5XX	MB88P552H -PF-5XX
ROM Size	8Kx8 bits	6Kx8 bits	8Kx8 bits	6Kx8 bits	8Kx8 bits	6Kx8 bits
	(On-chip One Time Programmable ROM)					
RAM Size (Directly address-ed locations)	256 x 4 bits (0-7)					
I/O Port:	Total 68 lines					
-Input only port	0					
-Output only port	0					
-I/O port	68					
-Control port	5 (Including serial I/O)					
Output Port Type	Standard pull-up		High-current open-drain		Standard pull-up Standard open-drain High-current open-drain	
Stack Depth (Nesting level)	8 levels					
Timer/Counter: -Buffer size -Clock source	Yes (Auto loading) 8 bits Internal/External					
Serial I/O: -Buffer size -Clock source -Output latch	Yes 4/8 bits Internal/External Yes					
Clock Generator: -Oscillator type	Yes Crystal/External (Fixed)				Yes Crsytal/Exteranl RC-Network/External (Option)	
-Clock Frequency (With prescaler)	- (1 MHz-8 MHz)				0.5 MHz - 4 MHz (1 MHz - 8 MHz)	
Clock Prescaler (Divid-by-two)	Yes (Fixed)				Yes/No (Option)	
Interrupt Function -Nesting level -Interrupt sources	Yes Single level 4 sources					
Programmable Pulse Generator	Yes (9 bit)					
A/D Converter: -Method -Resolution -Channel	Yes Programmable successive approximation 5 bit 4 channel					
Standby Function: -Initiation method -Oscillator state during standby -Output state during standby -Standby off reset function	No - - - -				Yes/No (Option) Software Idle/Stop (Soft-ware selectable) Hold/High-Z (Option) Yes/No (Option)	

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

Table 8: MB88P505H PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88P551H -PF-201	MB88P552H -PF-201	MB88P551H -PF-202	MB88P552H -PF-202	MB88P551H -PF-5XX	MB88P552H -PF-5XX
Output Port Level During Reset	High (Fixed)				High/Low (Option)	
Watch Dog Timer Function	No (Fixed)				Yes/No (Option)	
Number of Instructions	82					
Instruction Length/Cycle	1/1, 2/2, 2/3, or 3/3					
Min. Instruction Execution Time	1.5 µs at 8 MHz (With prescaler)					
Power Supply(VCC): –Active –Standby	+5V · 4.5V to 5.5V · 3.5V to 6.0V					
Programming Power Supply(PVCC)	17.5V to 18.5V					
Operating Temp. Range:	–30°C to +70°C					
Process	CMOS					
Package	80-pin plastic flat package					
Development Tools: –Hardware	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-36A : DUE board MB2115-100 : OTPROM writer with RS-232C interface MB2115-101 : Socket adapter for MB88P551H/552H					
–Software	SM05215-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-XXXX: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-XXXX: PC-DOS host emulator					

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ELECTRICAL CHARACTERISTICS

• ABSOLUTE MAXIMUM RATINGS†

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	
	V_{PP}	$V_{SS}-0.3$		$V_{SS}+21.0$	V	
	V_{SS} AVSS		0		V	
Input Voltage	V_{IN}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Output Voltage	V_{OUT}	$V_{SS}-0.3$		$V_{SS}+7.0$	V	Should not exceed $V_{CC}+0.3V$
Power Dissipation	P_D			600	mW	
Output Low Current	I_{OL}			20	mA	
Total I_{OL}	ΣI_{OL}			80	mA	
Operating Ambient Temperature	T_A	−30		+70	°C	
Storage Temperature	T_{STG}	−55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS
are exceeded. Functional operation should be restricted to the conditions
as detailed in the operational sections of this data sheet. Exposure to
absolute maximum rating conditions for extended periods may affect device
reliability.

• RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Guaranteed range
		3.5		6.0	V	Standby range
	V_{PP}	4.5	5.0	5.5	V	Normal operation mode
		17.5		18.5	V	Programming mode
Input High Voltage	V_{IH}	$0.7 \cdot V_{CC}$		$V_{CC}+0.3$	V	E-, R-Ports SI, PGI, EX(crystal/ceramic), PROG
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	V	$\overline{START}$, EX(RC−network), $\overline{IRQ}$, $\overline{TC}$, $\overline{SC/TO}$, $\overline{RESET}$,
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.3 \cdot V_{CC}$	V	E-, R-Ports SI, PGI, EX(crystal/ceramic),PROG
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	$\overline{START}$, EX(RC−netwarok), $\overline{IRQ}$, $\overline{TC}$, $\overline{SC/TO}$, $\overline{RESET}$
Operating Ambient Temperature	T_A	−30		+70	°C	

• **DC CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Min.	Typ.	Max.	Unit
Output High Voltage	V_{OH}	E-, R-Ports (Standard pull-up),	V_{CC}=4.5V I_{OH}=-200µA	2.4			V
		$\overline{X}$ (Selected by mask option)	V_{CC}=4.5V I_{OH}=-10µA	4.0			V
Output Low Voltage	V_{OL}	E-, R-Ports (All output option), $\overline{RESET}$,	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
		$\overline{X}$ (Selected by mask option)	V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		E-,R-Ports(High-current open-drain)	V_{CC}=4.5V I_{OL}=10mA			2.0	V
Input Leakage Current	I_{IH}	EX	V_{CC}=5.5V V_{IH}=5.5V			60	µA
	I_{IL}	E-, R-Ports (Standard pull-up)	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		EX, $\overline{RESET}$	V_{CC}=5.5V V_{IL}=0.4V			-60	µA
Open-drain Output Leakage Current	I_{LEAK}	E-,R-Ports(High-current/standard open-drain)	V_{CC}=5.5V V_{OH}=5.5V (N-ch. Tr off)		0.1	10	µA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	E-, R-Ports (High-Z during standby mode)	V_{CC}=6.0V(Standby) V_{IN}=0V to 6.0V			±25	µA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.) fc=2MHz(Operation) All outputs open		8		mA
	I_{CCH}	V_{CC} (Standby mode)	V_{CC}=6.0V(Max.) fc=0Hz(Standby) All outputs open			1.5	mA
	I_{PP}	V_{PP} (Programming mode)	V_{CC}=5.0V(Typ.) =5.5V(Max.) V_{PP}=18.0V fWCLK=20Hz All outputs open			30	mA
	I_{PP}	V_{PP} (Normal operation mode)	V_{CC}=5.0V(Typ.) =5.5V(Max.) V_{PP}=5.0V fc=1Hz(Opearation) All outputs open		1		mA
	I_{PPH}	V_{PP} mode)	V_{CC}=Vpp=6.0V f_C=0MHz(Stanbdy) All outputs open			10	µA
Input Capacitance	C_{IN}	All pins except V_{CC}, V_{SS}	fc=1MHz		10	20	pF

If standby function is selected by mask option, ICCH is different from mass-produced devices (MB88551H/2H).

- **AC CHARACTERISTICS**

  CLOCK TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_c	EX, X	Crystal/ceramic or RC-network	0.5	4	MHz	Without prescaler
			OSC, external clock drive Figs. 4 and 5	1	8		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 4 and 5	0.25	2	μs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive	100		ns	Without prescaler
			(with X open) Figs. 4 and 5	50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive (with X open) Figs. 4 and 5	5	200	ns	

Fig. 4: CLOCK TIMING

Fig. 5: CLOCK CIRCUIT CONFIGURATIONS

(1) Crystal/Ceramic Oscillation

(2) RC-Network * Oscillation

(3) External Clock Drive

* When the RC-network oscillation is used, the following conditions must be
  met: 1) The prescaler is not used.
       2) $V_{CC}=5V\pm10\%$
       3) $T_A=-30°C$ to $+70°C$
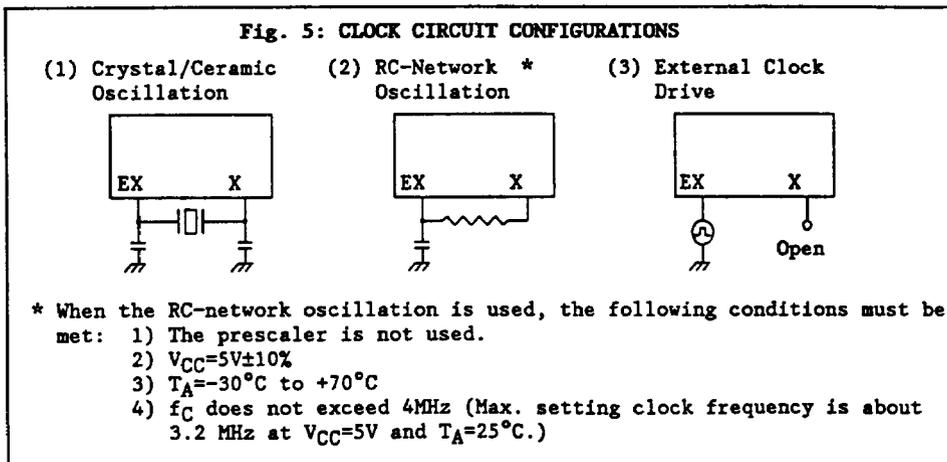   4) f_C does not exceed 4MHz (Max. setting clock frequency is about
          3.2 MHz at $V_{CC}=5V$ and $T_A=25°C$.)
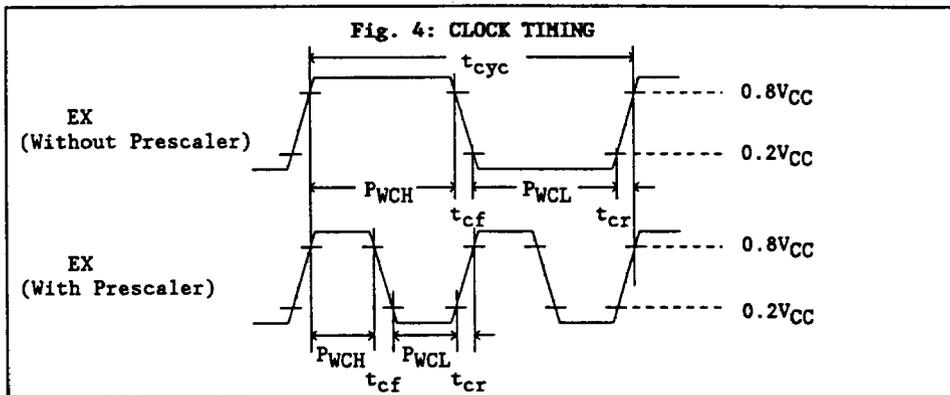
Fig. 6: RC-NETWORK OSCILLATION CHARACTERISTICS (EXAMPLE)

Oscillation Frequency f (MHz) vs External Capacitor C (pF)
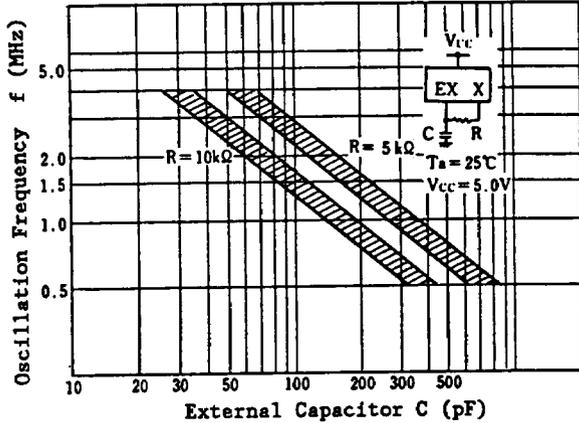
Note:
When the RC-network oscillations is used, the following conditions must be
met: 1) The prescaler is not used.   2) V_{CC}=5V±10%
      3) T_A=-30°C to 70°C   4) f_C does not exceed 4.0 MHz.

Fig. 7: CRYSTAL OSCILLATION CHARACTERISTICS (EXAMPLE)

Oscillation Frequency f (MHz) vs External Capacitor C1, C2 (pF)
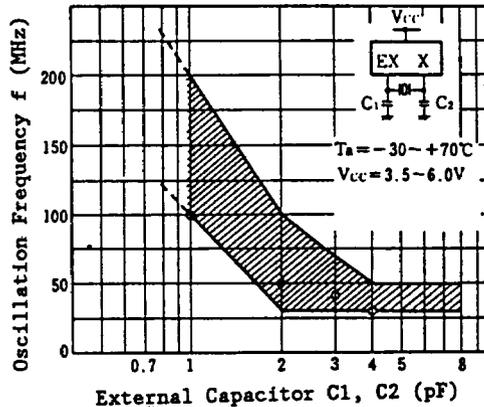
Notes:
1) The cross-hatched portion shows an area where the on-chip oscillator has
   stable oscillation characteristics and short oscillation stabilization time
   when an average crystal resonator is used. This chart gives an aim value of
   the external capacitor to realize a desired oscillation frequency. When an
   exact oscillation frequency is needed, a capacitor value should be deter-
   mined, adjusting to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency
   tend to have longer oscillation stabilization time and wider characteristic
   variations which affect on-chip oscillator characteristics. So, we recom-
   mend to use high-frequency crystal resonator with on-chip 1/2 prescaler.
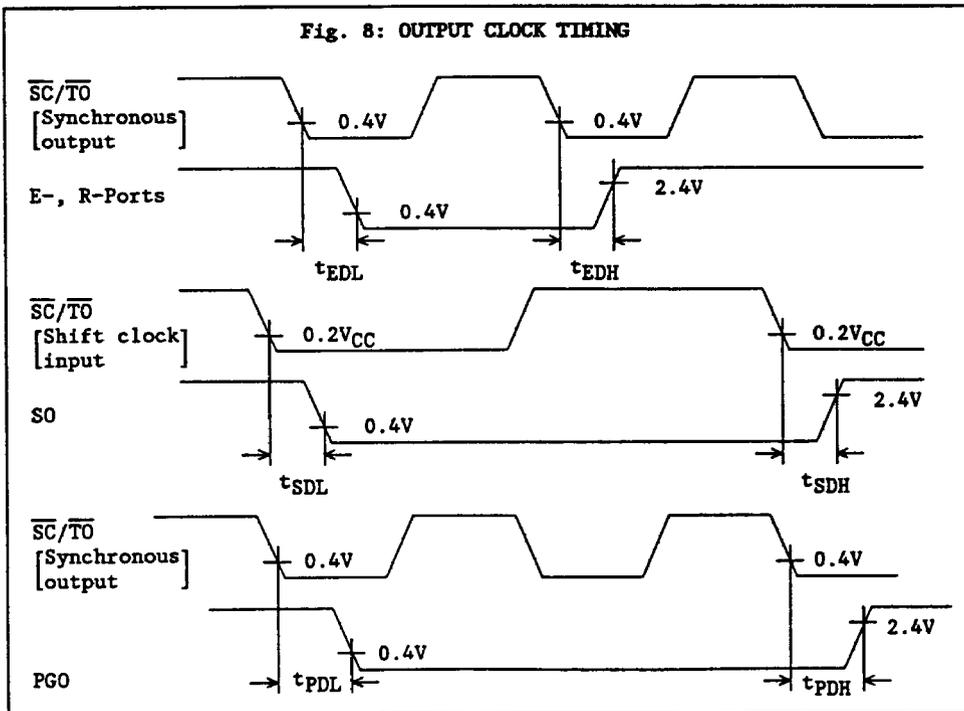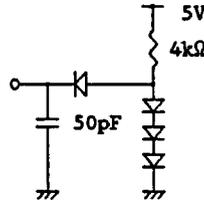
• **OUTPUT TIMING** (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
E-, R-Ports Delay Time	t_{EDH}	E-Port, R-Port	Fig. 8 *1		1000	ns
	t_{EDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 8		1000	ns
	T_{SDL}				350	
Pulse Generator Output Port Delay Time	t_{PDH}	PGO	Fig. 8		1000	ns
	T_{PDL}				350	

Note:
*1. A 10 kΩ pull-up is required when open-drain output is used.
*2. All the output loading values are 50 pF + 1TTL. See figure below.

Fig. 8: OUTPUT CLOCK TIMING

INPUT TIMING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	E-Port, R-Port	Fig. 9	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
SI Input Setup Time	t_{SDS}	SI	Fig. 9	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 9		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$2t_{cyc}-200$	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 9	$8t_{cyc}+50$		ns
		$\overline{IRQ}$		$2t_{cyc}+50$		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 9		$2t_{cyc}-200$	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 9	$2t_{cyc}+50$		ns
Pulse Generator Trigger Input Setup Time (synchronous mode)	t_{PS}	PGI	Fig. 9		$5t_{cyc}-200$	ns
Pulse Generator Trigger Input Hold Time (Synchronous mode)	t_{PH}	PGI	Fig. 9	$5t_{cyc}+50$		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 9	$6t_{cyc}+250$		ns
		$\overline{IRQ},\overline{TC},PGI$		$6t_{cyc}+250$		
		$\overline{RESET}$		$12t_{cyc}+250$		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 9	$12t_{cyc}+250$		ns
		$\overline{RESET}, \overline{TC}, \overline{IRQ}, PGI$		$6t_{cyc}+250$		
		START		500		
Control Signal Rise and Fall Time	$t_{CNr},$ t_{CNf}	START, $\overline{SC}/\overline{TO},\overline{IRQ},$ $\overline{RESET}, \overline{TC},$ PGI	Fig. 9	Should be less than 200ns		

3

FIG. 9: INPUT TIMING

$\overline{SC}/\overline{TO}$
[Synchronous output]

2.4V

0.4V

t_{DS}

- **Parallel Data Input**

$\leftarrow t_{DH}$

E-Port,
R-Port

$0.7V_{CC}$
$0.3V_{CC}$

- **Device Control Input**

t_{CNf} P_{WCNL} t_{CNr} P_{WCNH}

$\overline{IRQ}$,
$\overline{RESET}$,
START

$0.8V_{CC}$
$0.2V_{CC}$

t_{CH}

- **$\overline{TC}$ Input**

t_{CS}

$0.8V_{CC}$
$0.2V_{CC}$

t_{TS} t_{TH}

- **Serial Data Input**

t_{CNf} t_{CNr} P_{WCNH}

$\overline{SC}/\overline{TO}$
[Shift clock input]

P_{WCNL}

$0.8V_{CC}$
$0.2V_{CC}$

t_{SDS} t_{SDH}

SI

$0.7V_{CC}$
$0.3V_{CC}$

- **Pulse Generator Input**

$\overline{SC}/\overline{TO}$
[Synchronous output]

0.4V

2.4V

0.4V

t_{PS} t_{PH}

PGI

$0.7V_{CC}$
$0.3V_{CC}$

$\dfrac{P_{WCNH}}{P_{WCNL}}$

- **POWER-ON RESET**

Parameter	Symbol	Condi-tions	Value Min.	Value Max.	Unit	Remarks
Power Supply Rise Time	t_r	Fig. 10	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 10	1		ms	Required for accurate circuit operation repeatability
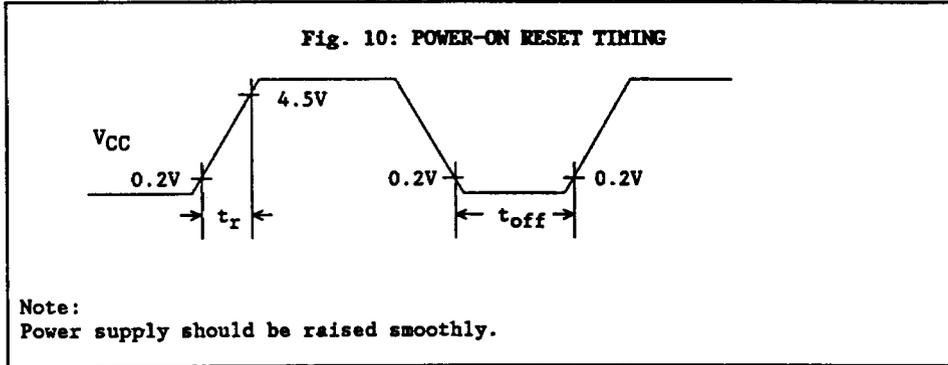
Fig. 10: POWER-ON RESET TIMING

Note:
Power supply should be raised smoothly.

3

- **A/D CONVERTER CHARACTERISTICS**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Resolution						5	Bit
Linearity Error			$T_A=25°C$ $V_{CC}=5.0V$			±1.0	LSB
Differential Linearity Error						±0.9	LSB
Zero Transition Voltage	V_{OT}			8	78	148	mV
Full-Scale Transition Voltage	V_{FST}			+4696	+4766	+4836	mV
Conversion Time			108 x t_{CYC}	27 *1		216*2	μs
Analog Port Input Current	I_{AIN}	AN3-0				5	μA
Analog Input Voltage		AN3-0		AV_{SS}		V_{CC}	V
Reference Voltage Supply Current		AV_{SS}		0	0	0	mA

Notes:
1. Error between analog inputs is within 1/2 LSB when $V_{CC}-AV_{SS}=5.0V$
~~2. Full scale and offset can be adjust by an appropriate setting of AV_R~~
2.~~5~~. Error becomes relatively larger as $|V_{CC}-AV_{SS}|$ becomes smaller.

*1 fc=8.0 MHz (with prescaler)
*2 fc=0.5 MHz (without prescaler)

- **Resolution**
  The minimum variation in an analog signal that can be discriminated by the A/D converter. (An analog voltage can be divided into $2^5=32$ parts.)
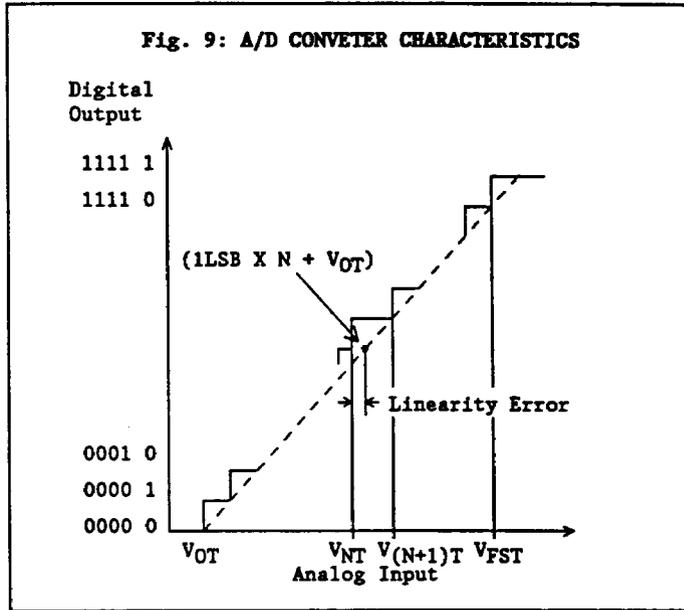
- **Linearity Error**
  The difference between the line connecting the device zero transition point ("0 0000" ⟷ "0 0001") with the full scale transition point ("1 1111" ⟷ "1 1110"), the actual conversion characteristics.

- **Differential Linearity Error**
  The difference from ideal input voltage required to change the output voltage code by 1LSB.

• A/D CONVERTER CHARACTERISTICS

Fig. 9: A/D CONVETER CHARACTERISTICS

Digital
Output

1111 1
1111 0

$(1LSB \times N + V_{OT})$

Linearity Error

0001 0
0000 1
0000 0

V_{OT} V_{NT} $V_{(N+1)T}$ V_{FST}
                 Analog Input

$$1LSB = \frac{V_{FST} - V_{OT}}{30}$$

$$\text{Linearity Error} = \frac{V_{NT} - (1\ LSB \times N + V_{OT})}{1\ LSB} \quad (LSB)$$

$$\text{Differential Linearity Error} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1 \quad (LSB)$$

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PACKAGE DIMENSION

• MB88P551H-PF/MB88P552H-PF: 80-PIN PLASTIC FLAT PACKAGE

80-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-80P-M01)

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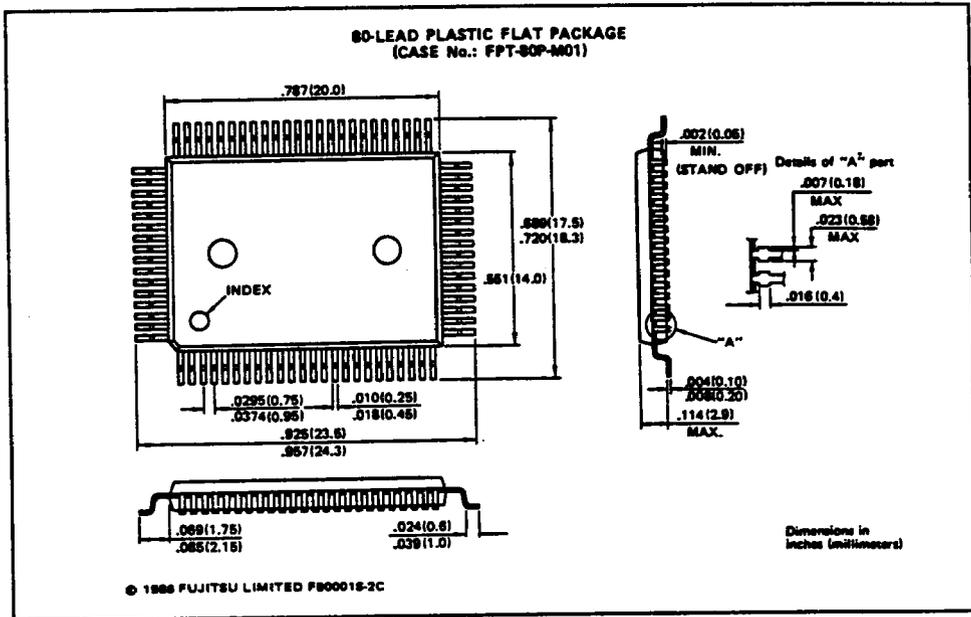
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