### INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# **74HC/HCT373**Octal D-type transparent latch; 3-state

Product specification
File under Integrated Circuits, IC06

September 1993





# Octal D-type transparent latch; 3-state

### 74HC/HCT373

### **FEATURES**

- 3-state non-inverting outputs for bus oriented applications
- · Common 3-state output enable input
- Functionally identical to the "563", "573" and "533"
- · Output capability: bus driver
- I<sub>CC</sub> category: MSI

### **GENERAL DESCRIPTION**

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE)

input and an output enable  $(\overline{OE})$  input are common to all latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the latches.

The "373" is functionally identical to the "533", "563" and "573", but the "563" and "533" have inverted outputs and the "563" and "573" have a different pin arrangement.

### **QUICK REFERENCE DATA**

 $GND = 0 \text{ V}; T_{amb} = 25 \, ^{\circ}\text{C}; t_r = t_f = 6 \text{ ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYP	ICAL	UNIT
	PARAMETER	CONDITIONS	нс	нст	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V			
	D <sub>n</sub> to Q <sub>n</sub>		12	14	ns
	LE to Q <sub>n</sub>		15	13	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	45	41	pF

### **Notes**

- 1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):
  - $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:
  - f<sub>i</sub> = input frequency in MHz
  - $f_o$  = output frequency in MHz
  - $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$
  - C<sub>L</sub> = output load capacitance in pF
  - $V_{CC}$  = supply voltage in V
- 2. For HC the condition is  $V_1 = \text{GND}$  to  $V_{CC}$ . For HCT the condition is  $V_1 = \text{GND}$  to  $V_{CC} 1.5 \text{ V}$

### **ORDERING INFORMATION**

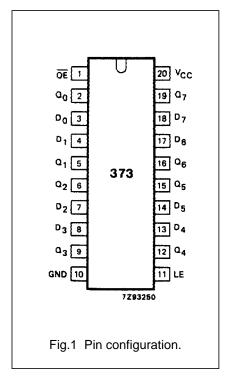
See "74HC/HCT/HCU/HCMOS Logic Package Information".

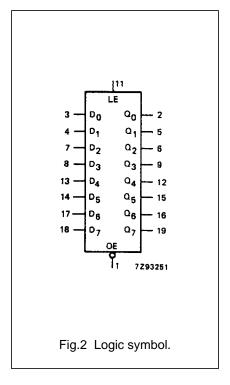
# Octal D-type transparent latch; 3-state

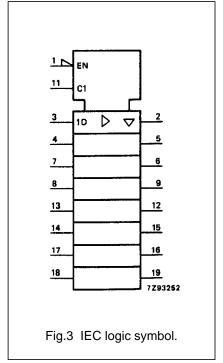
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### **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ŌĒ	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q <sub>0</sub> to Q <sub>7</sub>	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V <sub>CC</sub>	positive supply voltage

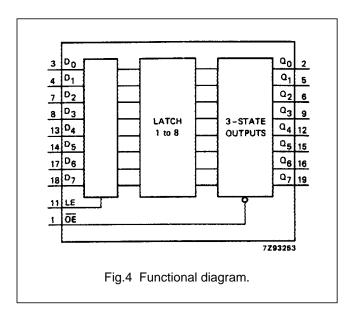


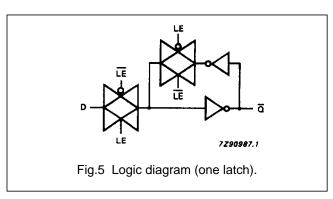




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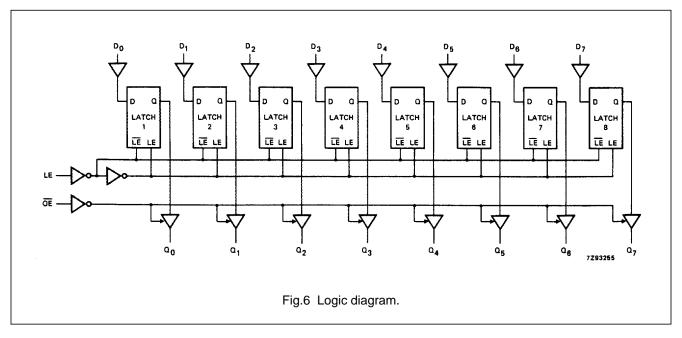


### **FUNCTION TABLE**

OPERATING	II.	IPUT	S	INTERNAL	OUTPUTS		
MODES	ŌΕ	LE	D <sub>n</sub>	LATCHES	Q <sub>0</sub> to Q <sub>7</sub>		
enable and read	L	Н	L	L	L		
register (transparent mode)	L	Н	Н	Н	Н		
latch and	L	L	I	L	L		
read register	L	L	h	Н	Н		
latch register and disable	H H	X X	X X	X X	Z Z		
outputs							

### **Notes**

- 1. H = HIGH voltage level
  - h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
  - L = LOW voltage level
  - I = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
  - X = don't care
  - Z = high impedance OFF-state



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### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

### **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

		T <sub>amb</sub> (°C)								TEST CONDITIONS	
CVMDOL	PARAMETER	74HC							] 		
SYMBOL		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub>	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(•)	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $Q_n$		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.7
t <sub>W</sub>	LE pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.10
t <sub>h</sub>	hold time D <sub>n</sub> to LE	5 5 5	-8 -3 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.10

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### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.30
LE	1.50
ŌE	1.00

### **AC CHARACTERISTICS FOR 74HCT**

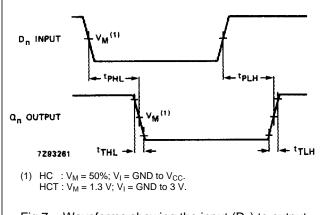
 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

		T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL	PARAMETER	74HCT									WAVEFORMS
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(-,	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		17	30		38		45	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to Q <sub>n</sub>		16	32		40		48	ns	4.5	Fig.8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time <del>OE</del> to Q <sub>n</sub>		19	32		40		48	ns	4.5	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time <del>OE</del> to Q <sub>n</sub>		18	30		38		45	ns	4.5	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.7
t <sub>W</sub>	LE pulse width HIGH	16	4		20		24		ns	4.5	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	12	6		15		18		ns	4.5	Fig.10
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4	-1		4		4		ns	4.5	Fig.10

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### **AC WAVEFORMS**



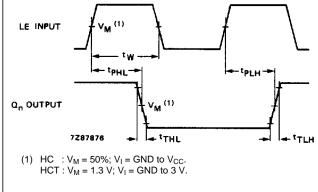
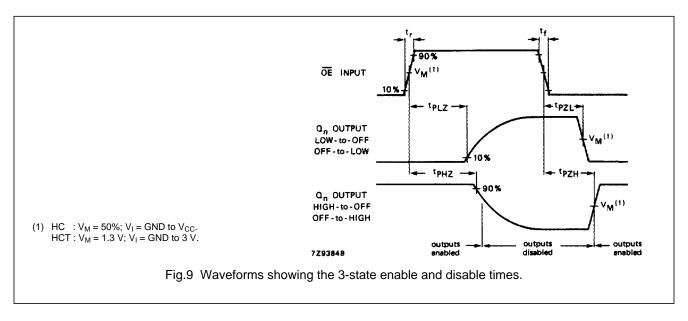
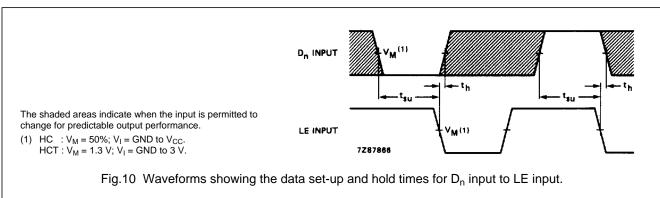


Fig.8 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q<sub>n</sub>) propagation delays and the output transition times.

Fig.7 Waveforms showing the input  $(D_n)$  to output  $(Q_n)$  propagation delays and the output transition times.





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### **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".