DATA SHEET

TDA4850
Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

Product specification
Supersedes data of September 1991
File under Integrated Circuits, IC02

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Philips
Semiconductors

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Horizontal and vertical deflection controller for VGA/XGA and multi-frequency monitors

TDA4850

FEATURES

- VGA operation fully implemented including alignment-free vertical and E/W amplitude pre-settings
- 4th VGA mode easy applicable (XGA, Super VGA)
- Multi-frequency operation externally selectable
- All adjustments DC-controllable
- Alignment-free oscillators
- Sync separators for video or horizontal and vertical TTL sync levels regardless of polarity
- Horizontal oscillator with PLL1 for sync and PLL2 for flyback
- Constant vertical and E/W amplitude in multi-frequency operation
- DC-coupling to vertical power amplifier (TDA486X or TDA8351)
- Internal supply voltage stabilization with excellent ripple rejection to ensure stable geometrical adjustments.

GENERAL DESCRIPTION

The TDA4850 provides economical solutions in VGA/XGA and multi-frequency monitors. The IC incorporates the complete horizontal and vertical small signal processing. VGA-dependent mode detection and settings are performed on chip. In conjunction with TDA486X or TDA8351 (vertical output circuits) both ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)	9.2	12	16	V
I_P	supply current	–	40	–	mA
$V_{i\ sync}$	AC-coupled composite video signal with negative-going sync (peak-to-peak value; pin 9)	–	1	–	V
	sync slicing level	–	120	–	mV
	DC-coupled TTL-compatible horizontal sync signal (peak value; pin 9)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
	DC-coupled TTL-compatible vertical sync signal (peak value; pin 10)	1.7	–	–	V
	slicing level	1.2	1.4	1.6	V
$I_{o\ V}$	vertical differential output current (peak-to-peak value; pins 5 and 6)	–	1	–	mA
$I_{o\ H}$	horizontal sink output current on pin 3	–	–	60	mA
T_{amb}	operating ambient temperature	0	–	70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4850	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

BLOCK DIAGRAM

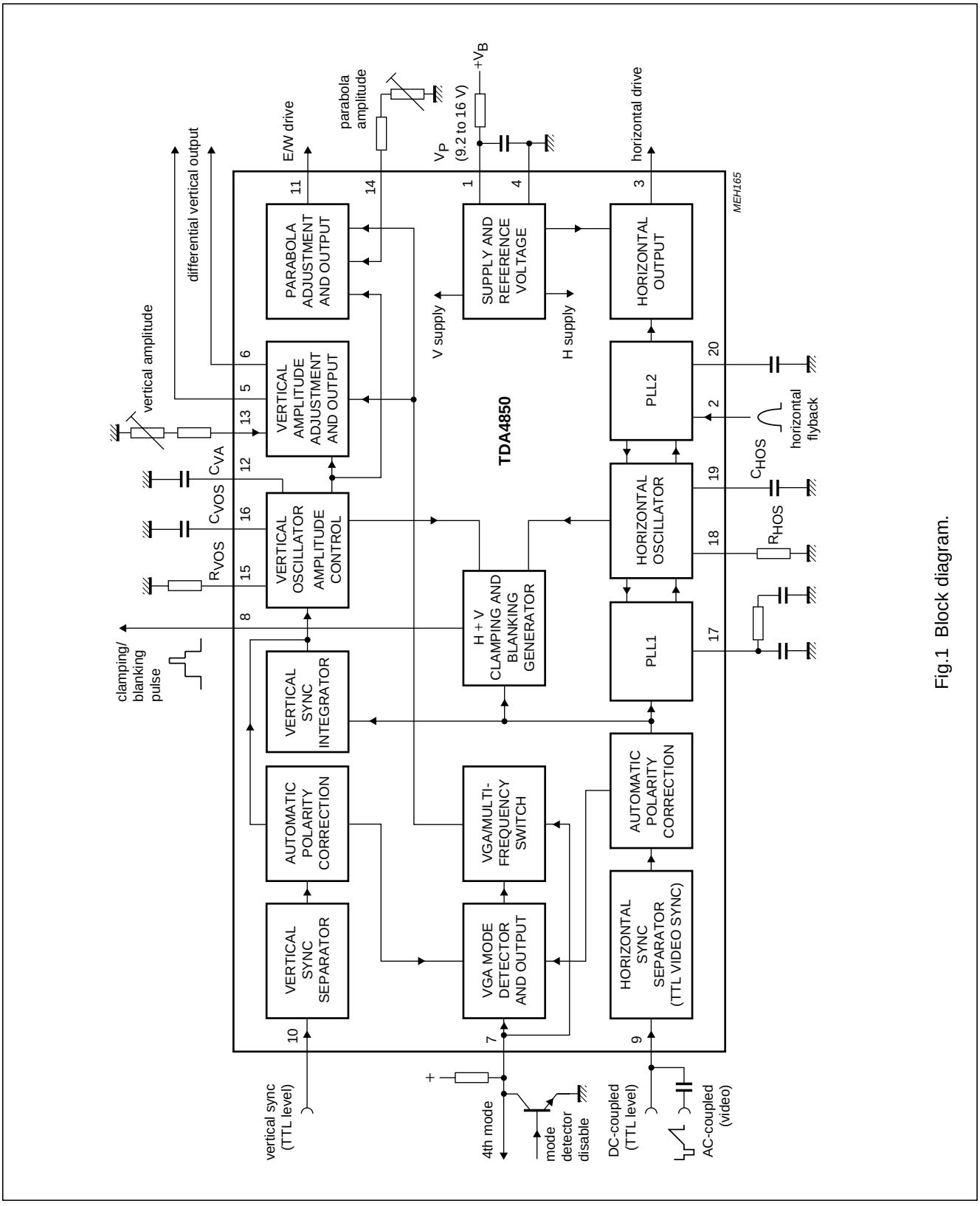


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
FLB	2	horizontal flyback input
HOR	3	horizontal output
GND	4	ground (0 V)
VERT1	5	vertical output 1; negative-going sawtooth
VERT2	6	vertical output 2; positive-going sawtooth
MODE	7	4th mode output and mode detector disable input
CLBL	8	clamping/blanking pulse output
HVS	9	horizontal sync/video input
VS	10	vertical sync input
EW	11	E/W output (parabola to driver stage)
C_{VA}	12	capacitor for amplitude control
R_{VA}	13	vertical amplitude adjustment input
R_{EW}	14	E/W amplitude adjustment input (parabola)
R_{VOS}	15	vertical oscillator resistor
C_{VOS}	16	vertical oscillator capacitor
PLL1	17	PLL1 phase
R_{HOS}	18	horizontal oscillator resistor
C_{HOS}	19	horizontal oscillator capacitor
PLL2	20	PLL2 phase

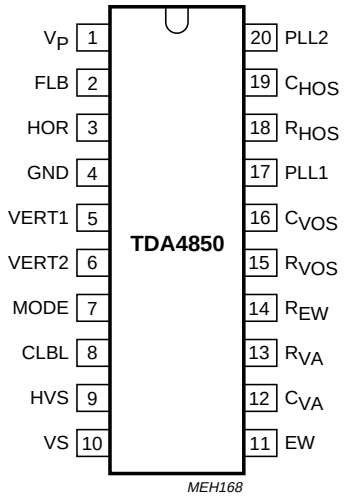


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Horizontal sync separator and polarity correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on pin 9. Video signals are clamped with top sync on 1.28 V, and are sliced at 1.4 V. This results in a fixed absolute slicing level of 120 mV related to top sync.

DC-coupled TTL sync signals are also sliced at 1.4 V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected.

The polarity information is fed to the VGA mode detector. The corrected sync is input signal for the vertical sync integrator and the PLL1 stage.

Vertical sync separator, polarity correction and vertical sync integrator

DC-coupled vertical TTL sync signals may be applied to pin 10. They are sliced at 1.4 V. The polarity of the separated sync is detected by internal integration, then polarity is corrected. The polarity information is fed to the VGA mode detector. If pin 10 is not used, it must be connected to ground.

The separated $V_{i(sync)}$ signal from pin 10, or the integrated composite sync signal from pin 9 (TTL or video) triggers directly the vertical oscillator.

VGA mode detector and mode output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V_P to pin 7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by HIGH on pin 7. This signal can be used externally to switch any horizontal or vertical parameters.

VGA mode detector input

For multi-frequency operation the voltage on pin 7 must be externally forced to a level of <50 mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 to 300 μs (575 μs is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 to 110 Hz.

Clamping and blanking generator

A combined clamping and blanking pulse is available on pin 8 (suitable for the video preamplifier TDA4880). The lower level of 2.1 V can be the blanking signal derived from line flyback, or the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals to the delay between vertical sync and start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA as well as for multi-frequency operation (selectable via pin 7).

The upper level of 3.9 V is the horizontal clamping pulse with internally fixed pulse width of 1 μs. A mono flop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse.

PLL1 phase detector

The phase detector is a standard one using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to pin 17.

Horizontal oscillator

This oscillator is a relaxation type oscillator. Its frequency is determined mainly by the capacitor on pin 19.
A frequency range of one octave is achieved by the current on pin 18. The φ1 control voltage from pin 17 is fed via a buffer amplifier and an attenuator to the current reference pin 18 to achieve a high DC loop gain. Therefore, changes in frequency will not affect the phase relationship between horizontal sync pulses and line flyback pulses.

PLL2 phase detector

This phase detector is similar to the PLL1 phase detector. Line flyback signals (pin 2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustments is possible by injecting a DC current from an external source into the PLL2 filter capacitor on pin 20.

Horizontal driver

This open-collector output stage (pin 3) can directly drive an external driver transistor. The saturation voltage is 300 mV at 20 mA. To protect the line deflection transistor, the horizontal output stage does not conduct at $V_P < 6.4$ V (pin 1).

Vertical oscillator and amplitude control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions.
The free-running frequency f_o is determined by the values of R_{VOS} and C_{VOS}. The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS}. Therefore, the oscillator frequency must be determined only by C_{VOS} on pin 16.

$$f_o = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_o (without adjustment) must be lower than the lowest occurring sync frequency. The contributions shown in Table 1 can be assumed.

Table 1 Calculation of f_o total spread

CONTRIBUTING ELEMENTS	%
Minimum frequency offset between f_o and the lowest trigger frequency	10
Spread of IC	±3
Spread of R (22 kΩ)	±1
Spread of C (0.1 μF)	±5
Total	19

Result for 50 to 110 Hz application: $f_o = \frac{50\ \text{Hz}}{1.19} = 42\ \text{Hz}$

Table 2 VGA modes

MODE	HORIZONTAL/VERTICAL SYNC POLARITY	HORIZONTAL FREQUENCY (kHz)	VERTICAL FREQUENCY (Hz)	NUMBER OF ACTIVE LINES	MODE OUTPUT PIN 7
1	+/–	31.45	70	350	LOW
2	–/+	31.45	70	400	LOW
3	–/–	31.45	60	480	LOW
4	+/+	fixed by external circuitry	–	–	HIGH

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)		–0.5	+16	V
$V_{3,7}$	voltage on pins 3 and 7		–0.5	+16	V
V_8	voltage on pin 8		–0.5	+7	V
V_n	voltage on pins 5, 6, 9, 10, 13, 14 and 18		–0.5	+6.5	V
I_2	current on pin 2		–	±10	mA
I_3	current on pin 3		–	100	mA
I_7	current on pin 7		–	20	mA
I_8	current on pin 8		–	–10	mA
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic handling for all pins	note 1	–	±300	V

Note

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	65	K/W

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal mode detector output (VGA mode)						
V_7	output saturation voltage LOW (for modes 1, 2 and 3)	I_7 = 6 mA	–	0.275	0.33	V
	output voltage HIGH	mode 4	–	–	V_P	V
I_7	load current to force VGA mode-dependent vertical and parabola amplitudes	modes 1, 2 and 3	2	–	6	mA
	output current	mode 4	–	0	–	mA
VGA/multi-frequency mode switch						
V_7	input voltage LOW to force multi-frequency mode		0	–	50	mV
Horizontal comparator PLL1						
V_{17}	upper control voltage limitation		–	5.0	–	V
	lower control voltage limitation		–	1.2	–	V
I_{17}	control current	see Fig.3	–	±300	–	μA
Horizontal oscillator						
f_{osc}	centre frequency	R_{18} = 12 kΩ (pin 18); C_{19} = 2.2 nF (pin 19)	–	31.45	–	kHz
Δf_{osc}	deviation of centre frequency		–	–	±3.0	%
TC	temperature coefficient		–	–	±150	10^{-6}/K
φ_H/t_H	relative holding/catching range		±6	±6.5	±7.3	%
R_{18}	external oscillator resistor		9	–	18	kΩ
V_{18}	voltage at reference current input (pin 18)	PLL1 and PLL2 locked; V_{ref} = 6.25 V	–	3.125	–	V
ΔV_{18}	control voltage		–	±205	–	mV
Horizontal PLL2; see Fig.3						
V_2	upper clamping level of flyback input	I_2 = 6 mA	–	5.5	–	V
	lower clamping level of flyback input	I_2 = –1 mA	–	–0.75	–	V
	H-flyback slicing level		–	3.0	–	V
I_2	input current	H-scan; V_8 < 0.9 V	–0.5	–	–	mA
		H-flyback; V_8 > 1.8 V	–	–	–0.2	mA
t_d/t_H	delay between middle of sync and middle of H-flyback related to t_H		–	3.2	–	%
V_{20}	upper control voltage limitation		–	4.6	–	V
	lower control voltage limitation		–	1.6	–	V
I_{20}	control current		–	±200	–	μA
$\Delta t/t_H$	PLL2 control range related to t_H		30	–	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal output (open-collector); see Fig.3						
V_3	output voltage LOW	I_3 = 20 mA	–	–	0.3	V
		I_3 = 60 mA	–	–	0.8	V
t_p/t_H	t_H duty cycle		42	45	48	%
V_P	threshold to activate too low supply voltage protection	horizontal output off	–	5.3	–	V
		horizontal output on	–	5.6	–	V
Horizontal clamping/blanking generator output; see Fig.3						
V_8	output voltage LOW	H and V scanning	–	–	0.9	V
	blanking output voltage	internal V blanking	1.8	2.1	2.4	V
		external H blanking	1.8	2.1	2.4	V
	clamping output voltage	H-sync on pin 9	3.5	3.9	4.3	V
I_8	internal sink current for all output levels	H and V scanning	2.3	2.9	3.5	mA
t_8	clamping pulse start		with end of H-sync			
t_{clp}	clamping pulse width		0.8	1.0	1.2	µs
S	steepness of rise and fall times		–	40	–	ns/V
Vertical oscillator (V_{ref} = 6.25 V)						
f_o	vertical free-running frequency	R_{15} = 22 kΩ; C_{16} = 0.1 µF	40	42	43.3	Hz
f_V	nominal vertical sync range	no f_o adjustment	50	–	110	Hz
V_{15}	voltage on pin 15	R_{15} = 22 kΩ	2.8	3.0	3.2	V
t_d	delay between sync pulse and start of vertical scan	measured on pin 8				
	in VGA/XGA mode, activated by an external resistor on pin 7		500	575	650	µs
	in multi-frequency mode	V_7 < 50 mV	240	300	360	µs
I_{12}	control current for amplitude control		–	±200	–	µA
C_{12}	capacitor for amplitude control		–	–	0.33	µF
Vertical differential output; see Fig.4						
I_o	differential output current between pins 5 and 6 (peak-to-peak value)	mode 3; I_{13} > –135 µA; R_{15} = 22 kΩ	0.9	1.0	1.1	mA
	maximum offset current error	I_o = 1 mA	–	–	±2.5	%
	maximum linearity error		–	–	±1.5	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical amplitude adjustment (in percent of output signal)						
V_{13}	input voltage		–	5.0	–	V
I_{13}	adjustment current	$I_{o\ max}$ (100%)	–110	–120	–135	μA
		$I_{o\ min}$ (typically 58%)	–	0	–	μA
$\Delta I_o/\Delta t$	VGA mode-dependent pre-settings activated by an external resistor on pin 7	note 1; see Table 2				
	mode 1		116.1	116.8	117.5	%
	mode 2		102.0	102.2	102.5	%
	mode 3		–	100	–	%
	mode 4		–	100	–	%
	multi-frequency operation (VGA operation disabled)	V_7 < 50 mV	–	100	–	%
E/W output; note 2						
V_{11}	bottom output signal during mid-scan (pin 11)	internally stabilized	1.05	1.2	1.35	V
	top output signal during flyback		4.1	4.35	4.6	V
TC	temperature coefficient of output signal		–	–	250	10^{-6}/K
E/W amplitude adjustment (parabola); see Fig.4						
V_{14}	input voltage (pin 14)		–	5.0	–	V
I_{14}	adjustment current	100% parabola	–110	–120	–135	μA
		typically 28% parabola	–	0	–	μA

Notes to the Characteristics

1. $\Delta I_o/\Delta t$ relative to value of mode 3.
2. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to pin 14.

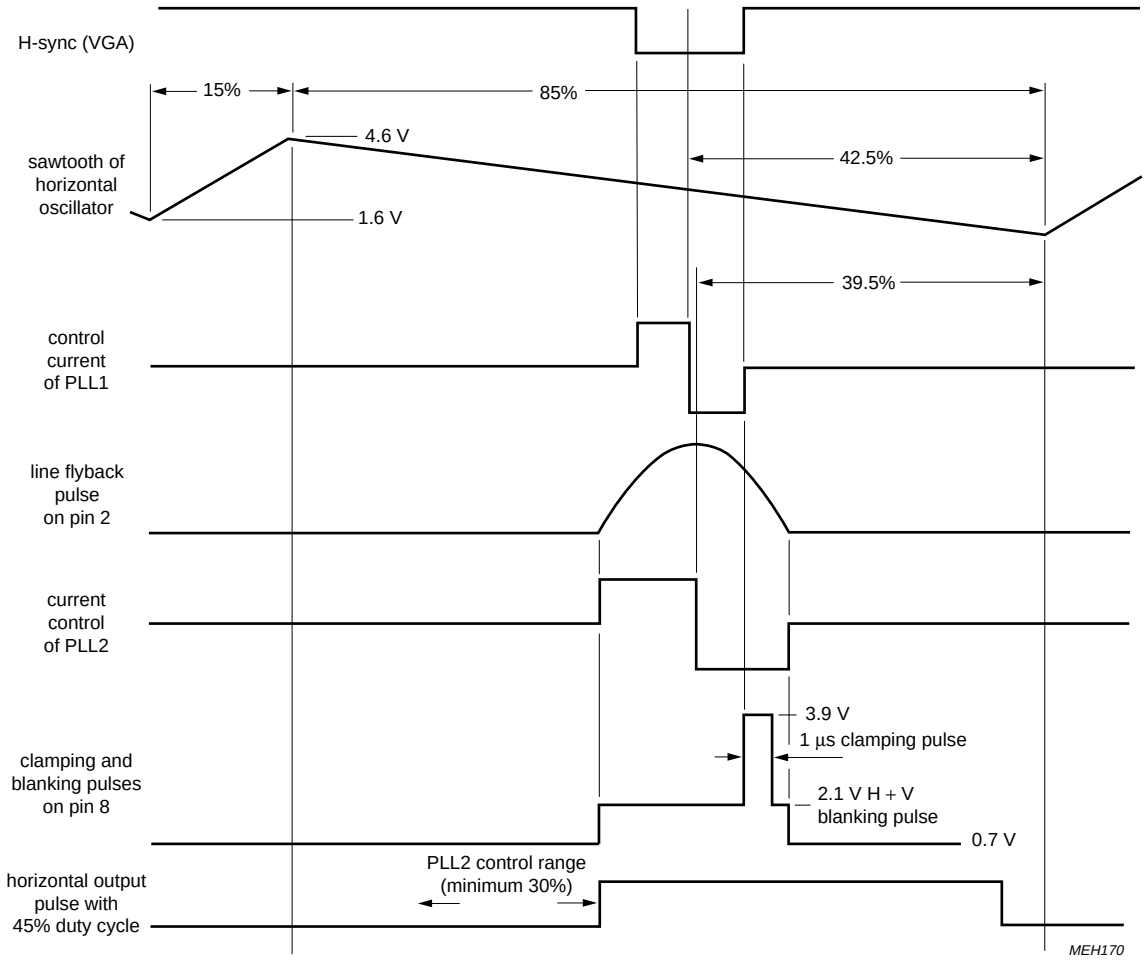
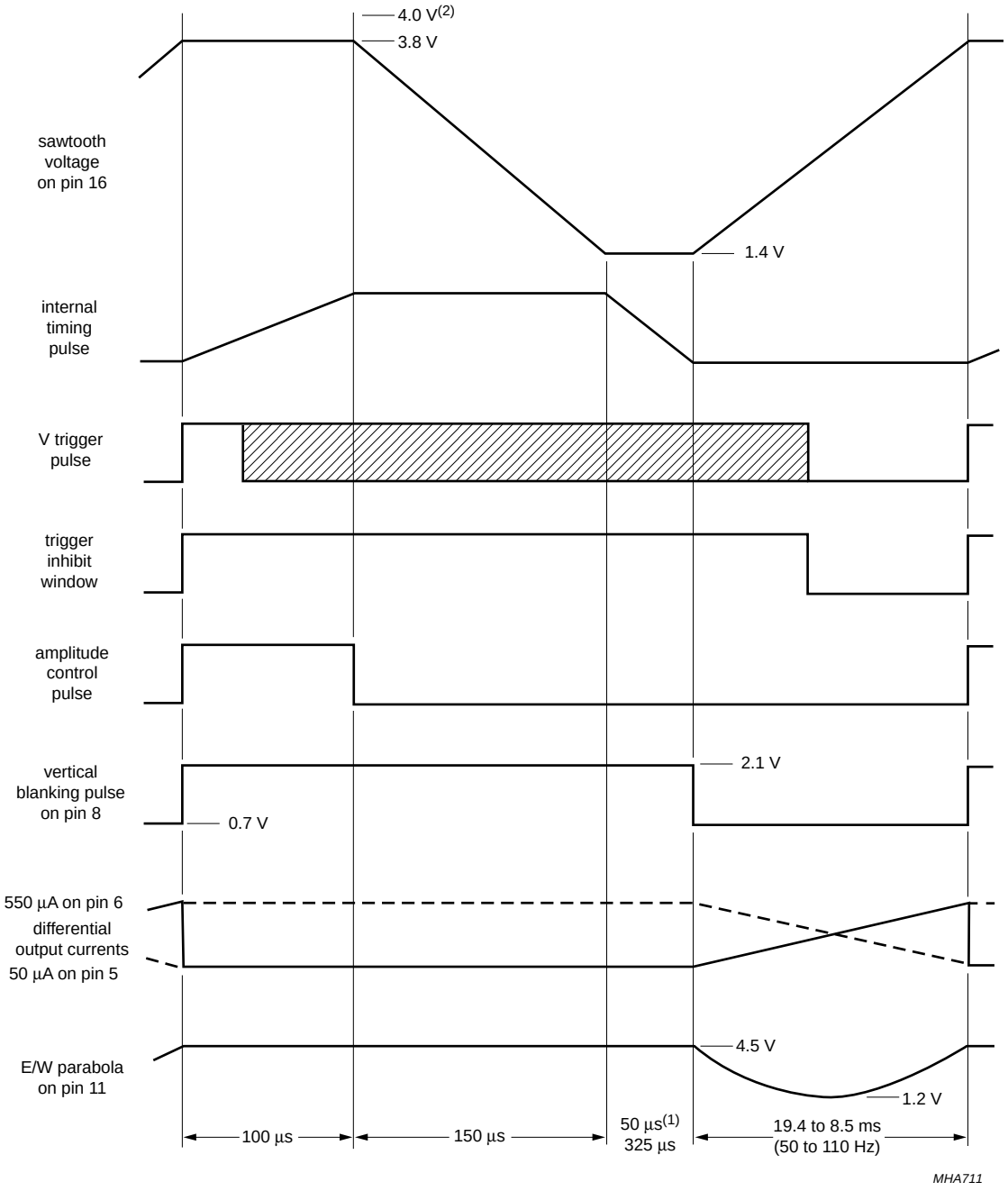


Fig.3 Horizontal timing diagram.



(1) In multi-frequency mode.
(2) For free-running oscillator.

Fig.4 Vertical and E/W timing diagram.

INTERNAL CIRCUITRY

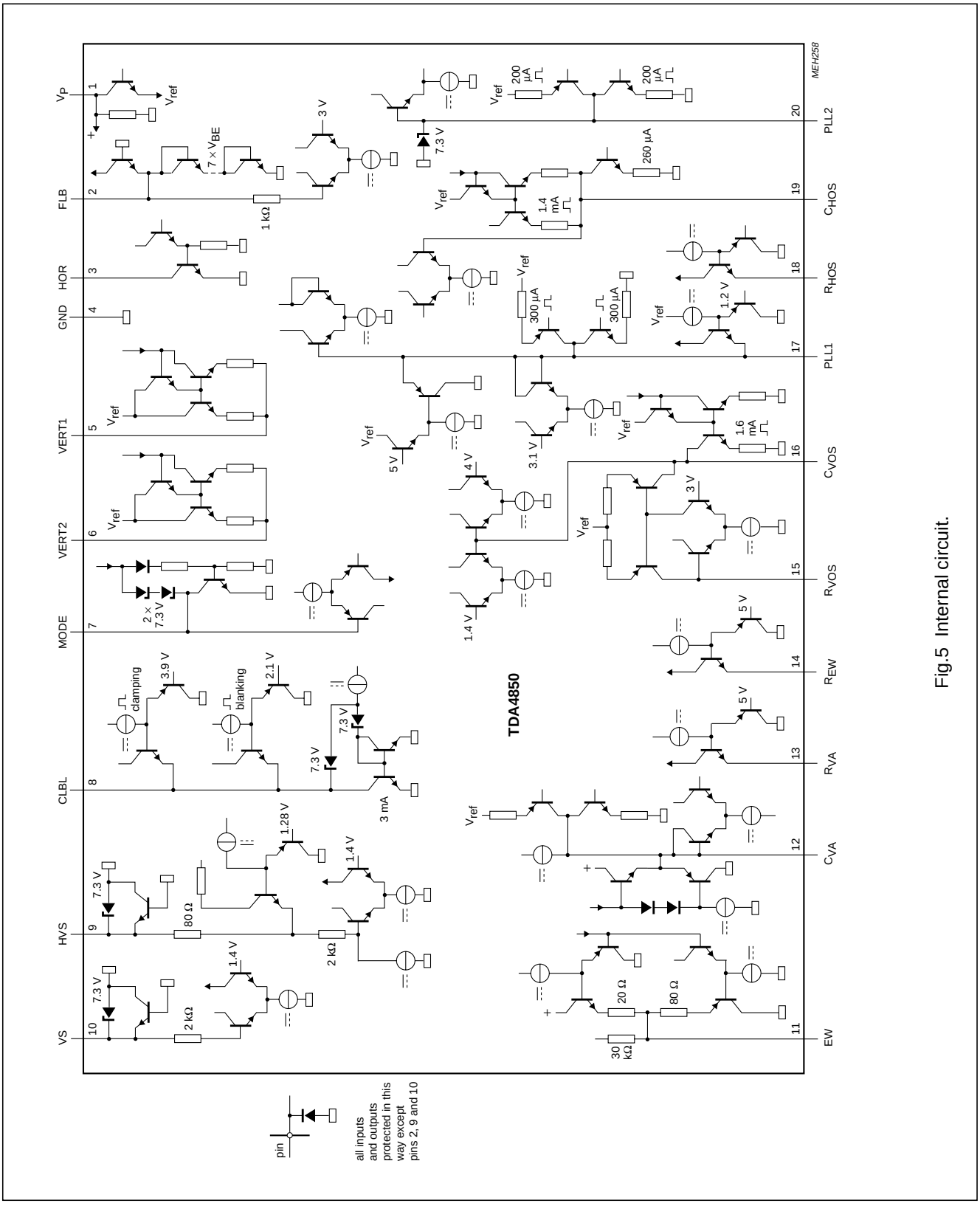


Fig.5 Internal circuit.

TEST AND APPLICATION INFORMATION

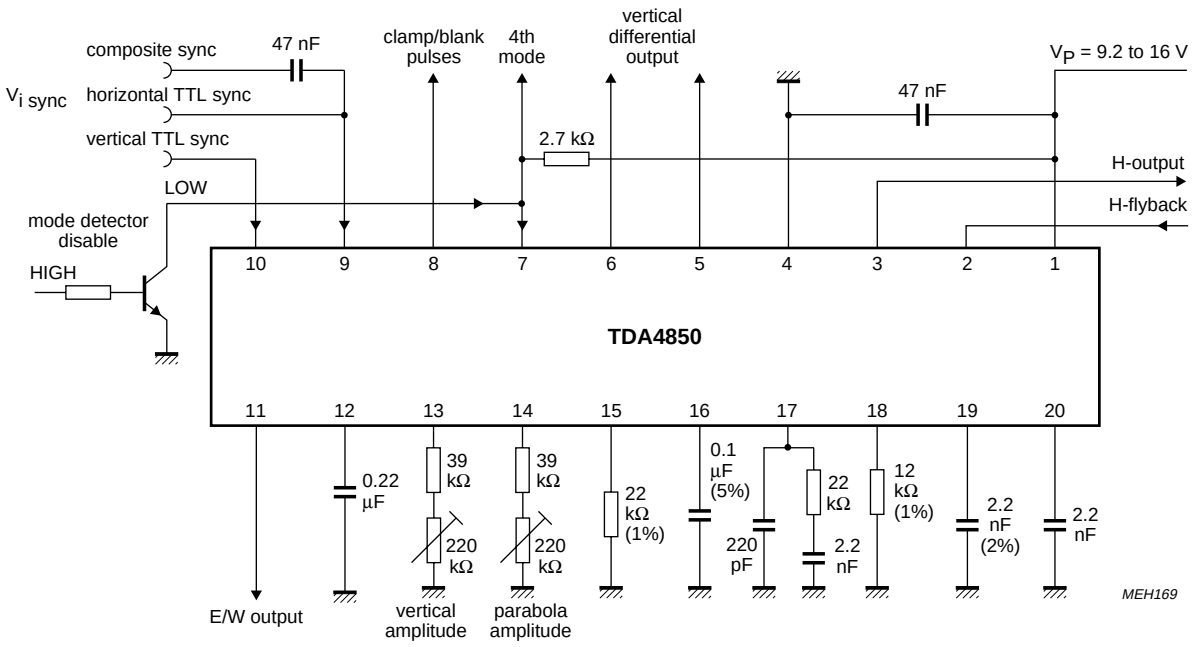
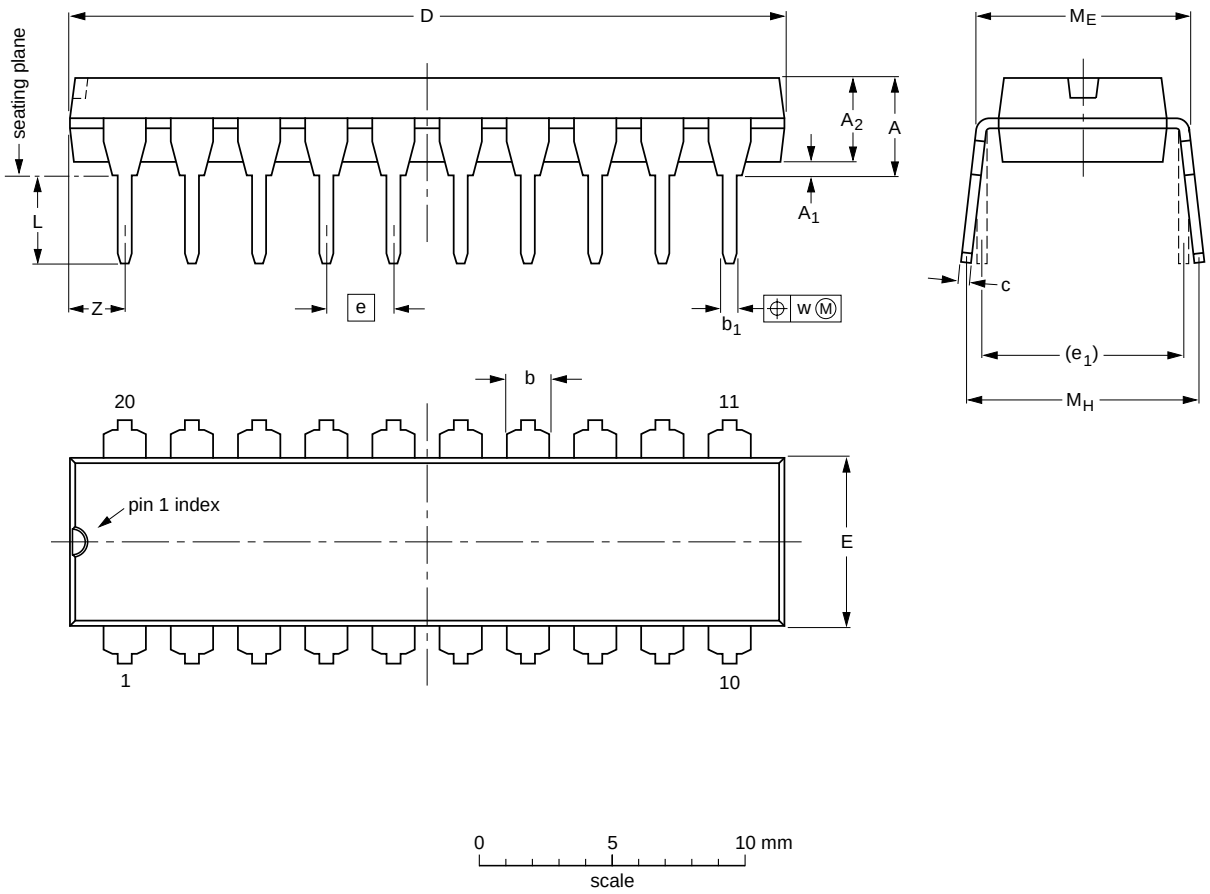


Fig.6 Test and application circuit (measurements taken at V_P = 12 V).

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale

NOTES

NOTES

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