DATA SHEET

TDA8349A
Multistandard IF amplifier and demodulator

Product specification
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Multistandard IF amplifier and demodulator

TDA8349A

GENERAL DESCRIPTION

The TDA8349A is a multistandard IF amplifier and demodulator with AGC and AFC functions for television receivers. The device has a video recognition circuit and a video switch for internal or external video for full SCART applications.

FEATURES

- Full-range gain-controlled wideband IF amplifier up to 60 MHz
- Wide-band video amplifier with good linearity and a class AB output stage to ensure a very low output impedance
- Supply independent video output level
- Small second harmonic IF output
- AGC circuit which operates on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC) with reduced sensitivity for high sound carriers
- AFC circuit with an internal 90° phase shift circuit, a sample-and-hold circuit for negatively modulated signals to reduce video dependent AFC information and an analog or digital output
- Video recognition possibility based on horizontal pulse duty cycles
- Video switch for selection of internal or external video signals
- Wide supply voltage range and ripple rejection
- Requires few external components
- Tuner AGC output for npn and pnp tuners

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current (pin 14)	V_i = 10 mV	40	55	65	mA
$V_{1-2(RMS)}$	IF input sensitivity (RMS value)		–	50	80	µV
G_v	IF gain control range		66	72	–	dB
$V_{11-17(p-p)}$	video output voltage (peak-to-peak value)		1.7	1.9	2.1	V
S/N	signal-to-noise ratio	V_i = 10 mV	54	61	–	dB
$V_{8-17(p-p)}$	AFC output voltage swing (peak-to-peak value)		10	–	11	V

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8349A	20	DIL	plastic	SOT146(1)

Note

1. SOT146-1; 1996 November 29.

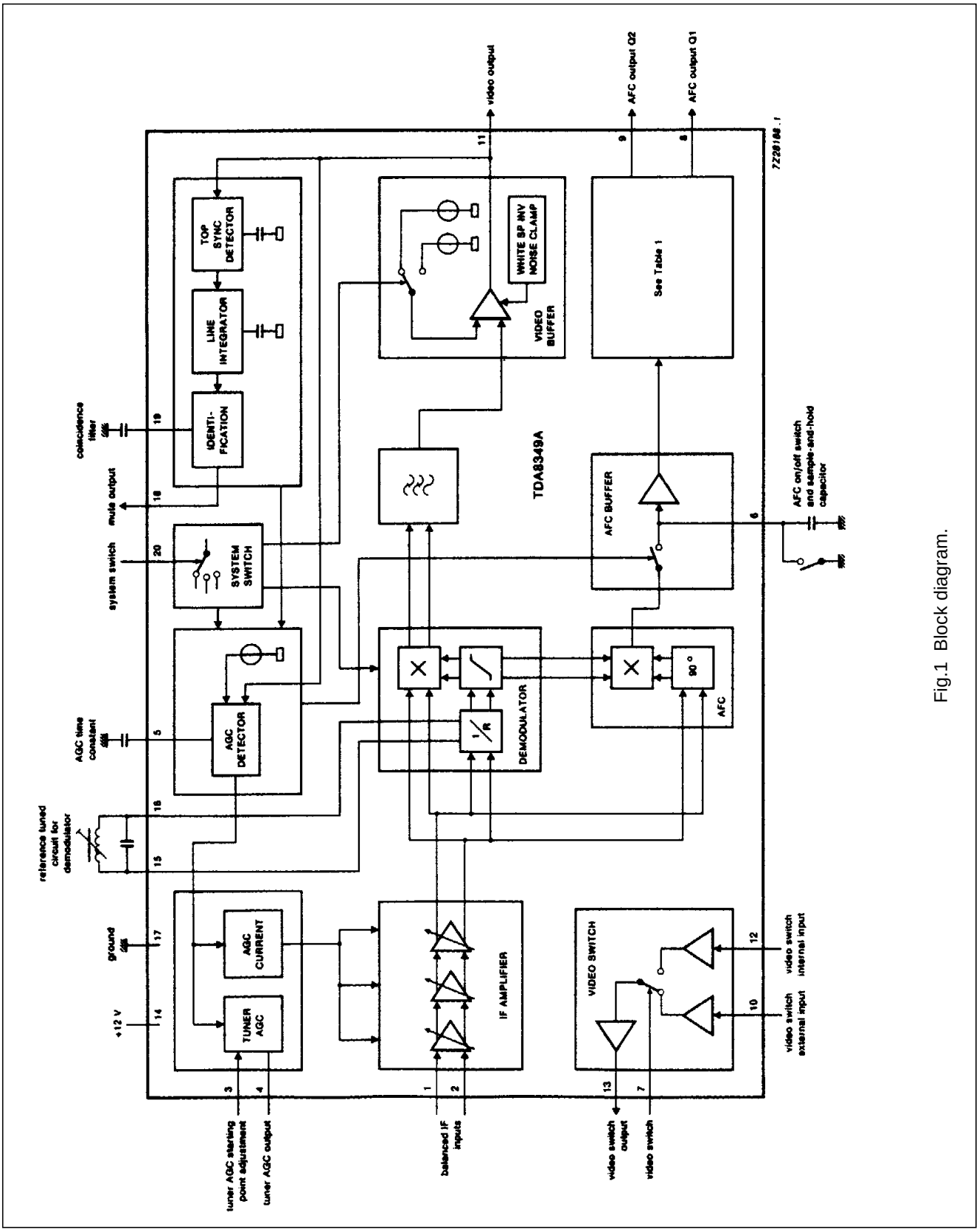


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1,2	balanced IF inputs
3	tuner AGC starting point adjustment
4	tuner AGC output
5	AGC time constant
6	AFC on/off switch and sample-and-hold capacitor
7	video switch
8	AFC output Q1
9	AFC output Q2
10	video switch external input
11	video output
12	video switch internal input
13	video switch output
14	positive supply voltage
15,16	reference tuned circuit for demodulator
17	ground
18	mute output
19	coincidence filter
20	system switch

FUNCTIONAL DESCRIPTION

General

The IC consists of the following parts as illustrated in Fig.1:

- Gain controlled video IF amplifier
- Quasi-synchronous demodulator
- Video amplifier/buffer with white spot clamp/inverter and noise clamp
- AGC circuit which operates either on top sync level (negative modulation) or on white level (positive modulation) or on top level (MAC)
- AFC circuit with sample-and-hold circuit for negatively modulated signals, on/off switch and a digital or analog output (switchable)
- Circuit for switching between positive and negative modulation
- Video recognition circuit for sound muting and tuning indication
- Video switch which facilitates selection between two different video signals, with different gain settings

IF amplifier

The IF amplifier consists of three AC coupled differential gain stages with adjustable feedback in the emitter. The AC coupling allows simple biasing, cascades can be used and no DC feedback is required. This provides a control range above 70 dB with good linearity. The minimum input signal to obtain the nominal output amplitude is 50 μV RMS.

Demodulator

The demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and a tuned circuit for selectivity. The regenerated carrier signal is limited by a clamping circuit before it is fed to the demodulator. Switching between positive and negative modulation is achieved by the system switch which provides currents to the demodulator in a positive or negative direction.

Video amplifier

The video amplifier based on the feedback principle improves the linearity of the video output buffer. It has an internal bandgap reference to ensure a stable video output at different supply voltages and temperatures. This

bandgap also reduces the supply ripple on the video output to values less than –30 dB. The video amplifier has a typical bandwidth of 10 MHz which allows application for all new video standards with bandwidths of up to 10 to 12 MHz. The video output signal has an amplitude of 2 V (p-p). White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers. A switchable DC shift for positively modulated IF signals ensures correct signal handling. This switching is obtained via pin 20, which is the same pin used for switching the demodulation polarity in the demodulator.
The circuit also has a noise clamp which prevents the video output becoming less than ±400 mV below the top sync level at noise peaks. The output buffer of the video amplifier consists of a class A/B circuit which can handle large source as well as large sink currents. This makes the circuit more flexible in several applications with one or more ceramic filters connected to this output buffer.

AGC control circuit

This converts the AGC detector voltage (pin 5) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted by a voltage between 3 and 5 V for pnp tuners and between 7 and 9 V for npn tuners via pin 3.

AGC circuit

A new AGC system has been designed for the AGC. It will be a top sync-detector for negatively modulated signals and a top white level AGC for positively modulated signals. For optimal flexibility reasons the load and unload currents of the AGC are chosen such that both, a relatively fast set, as well as a set with a low tilt are possible for positive (L) and negative (B/G) modulated signals. For this reason a tilt ratio between positive (L) and negative (B/G) of approximately 3:1 has been chosen. This means that in a fast set the choice of a typical tilt for negatively modulated signals of 2% will obtain a typical tilt for positively modulated signals (L) of 6%. For a digital set which requires a small tilt the choice of tilt can be a factor of 5 or 10 smaller by increasing the AGC capacitor.

The chosen AGC currents:

MODE	UNLOAD CURRENT	LOAD CURRENT	TILT AT 2.2 μF
B/G	50 μA	1.5 mA	typ. 0.5% (line tilt)
L	500 nA (note 1)	1.5 mA	typ. 1.5% (field tilt)
MAC(positive)	200 nA	1.5 mA	typ. 1.2% (frame tilt)
MAC(negative)	500 nA	1.5 mA	typ. 1.5% (field tilt)

Note

1. As long as no signal has been identified by the identification detector the unload current will be 50 μA.

Switching between the first three modes can be achieved by the system switch. This is a 3-level switch which when grounded selects B/G; open or 5 V selects L, and with pin 20 connected to V_{CC} selects positively modulated MAC. The IC operates in a fourth mode if the identification capacitor at pin 19 is connected to V_{CC}, it can be used for negatively modulated MAC.
During channel switching a situation can occur that requires the AGC to increase the gain more than for example 50 dB. If this increase of gain has to be done for a positively modulated (L) signal, it will be achieved by the 500 nA load current and is therefore extremely slow. Because the identification information can be used to indicate that the signal is too small, in this event the identification circuit will mute, it is possible to increase the positive unload current to the same value as that used for negatively modulated signals. This switching is fully automatic and cannot be switched off.

AFC circuit

The AFC circuit consists of a demodulator stage which is fed with signals 90° out of phase. A very accurate internally realized 90° phase shift circuit makes it possible to use the demodulator IF regenerator tuned circuit for tuning the AFC circuit. To prevent video ripple on the AFC output voltage a sample-and-hold circuit is used for negatively modulated signals. The output signal of the demodulator is sampled during sync level of the video signal and will be stored with the aid of an external capacitor.

This sample-and-hold circuit is not used in the L mode, but it will function as a low-pass filter in this mode and therefore also reduces the video dependency of the AFC. A gain stage amplifies the voltage swing by 5 times. The output of the AFC circuit will be an inverse analog output on pin 8 when pin 9 is connected to a voltage above 8 V. If pin 9 is connected to a voltage above 10 V the output will be a normal analog output. Normally pins 8 and 9 together provide digital AFC information.

Video recognition circuit

For full scart functions it is necessary to implement a second mute function for non-video signals in the whole television concept. This is realized in this IF-IC. With an internal sync separator and an internal integrator it is possible to achieve a very sensitive identification circuit, which measures the mean frequency of the input signal. This is normally approximately 16 kHz. The integrator capacitor will be loaded during the whole line time and unloaded during the sync pulse. The maximum voltage at this internal capacitor is a value for the main frequency of the video signal. By changing the value of an external capacitor it is possible to influence the speed and sensitivity of the recognition circuit. It is possible to gain sensitivity performance at disturbed signals by increasing the value of the external capacitor, however this will reduce the speed of the identification circuit.

Video switch circuit

The video switch also provides application for full SCART functions. The circuit has two inputs, one output and a control pin. The switch selects either internal or external video signals. A $\times 2$ gain stage for the external input provides an equal output level for internal or external video from the SCART. The crosstalk of the unwanted signal is better than –50 dB and the total signal handling meets all the requirements for SCART specifications.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{14\text{-}17}$	supply voltage (pin 14)	–0.5	13.2	V
P_{tot}	total power dissipation	–	1.2	W
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	–25	+ 75	°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; carrier frequency 38.9 MHz; negative modulation; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
supply						
V_{14-17}	supply voltage (pin 14)		10.2	12	13.2	V
I_{14}	supply current	V_i = 10 mV	40	55	65	mA
IF amplifier (note 1)						
V_{1-2}	input sensitivity	note 2	–	50	80	μV
R_{1-2}	differential input resistance	note 3	–	2	–	kΩ
C_{1-2}	differential input capacitance	note 3	–	2	–	pF
ΔG_{1-2}	gain control range		66	72	–	dB
ΔV_{11}	output signal for 50 dB input signal variation	note 4	–	0.5	–	dB
V_{1-2}	maximum input signal		100	–	–	mV
f_{1-2}	maximum operating frequency		60	–	–	MHz
Video output (note 5)						
	zero signal output level	note 6				
V_{11}	negative modulation		–	4.75	–	V
V_{11}	positive modulation		–	2.65	–	V
V_{11}	top sync level (top sync AGC)	note 7	–	2.7	–	V
V_{11}	white level (white level AGC)	note 8	–	4.6	–	V
$V_{11(p-p)}$	amplitude of video output signal (peak-to-peak value)		1.7	1.9	2.1	V
V_{11}	amplitude difference (positive/negative)		–	0	10	%
V_{11}	video output voltage variation	ΔV_P = 1 V	–	–30	–	dB
V_{11}	white spot threshold level	see Fig.3	–	5.6	–	V
V_{11}	white spot insertion level	see Fig.3	–	3.8	–	V
V_{11}	noise clamping level	see Fig.3	–	2.3	–	V
Z_{11}	output impedance		–	–	10	Ω
I_{11}	maximum sink current		5	–	10	mA
I_{11}	maximum source current		5	–	10	mA
B_{11}	bandwidth of demodulated output signal		7.5	10.0	–	MHz
G_d	differential gain	note 9	–	2	–	%
φ_d	differential phase	note 9	–	7	–	deg
Y_{nl}	luminance non-linearity	note 10	–	2	5	%
	intermodulation	see Figs 6 and 7				
α	1.1 MHz blue		–	–66	–	dB
α	1.1 MHz yellow		–	–60	–	dB
α	3.3 MHz blue		–	–60	–	dB
α	3.3 MHz yellow		–	–60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	signal-to-noise ratio	note 11				
S/N		V_i = 10 mV	54	61	–	dB
S/N		minimum gain	60	66	–	dB
$V_{1(rms)}$	residual carrier signal (RMS value)		–	10	20	mV
$V_{11(rms)}$	residual 2nd harmonic of carrier signal (RMS value)		–	3	10	mV
System switch (note 12)						
V_{20}	maximum voltage for mode B/G		1.4	–	–	V
I_{20}	input current	V_{20} = 0 V	–	–300	–	µA
V_{20}	minimum voltage for mode L		–	–	3	V
V_{20}	maximum voltage for mode L		7	–	–	V
I_{20}	input current	3 V ≤ pin 20 ≤ 7 V	–150	–	250	µA
V_{20}	minimum voltage for MAC (positive)		–	–	9.5	V
I_{20}	input current	$V_{20} = V_P$	–	500	–	µA
AGC control circuit						
t_{11}	response to an amplitude increase of 52 dB of the IF input with the AGC switched to mode B/G	note 13	–	2	–	ms
t_{11}	response to an amplitude decrease of 52 dB of the IF input with the AGC switched to mode B/G	note 14	–	25	–	ms
	allowed leakage current of the AGC capacitor					
I_5	top sync level AGC		–	10	–	µA
I_5	white level AGC		–	200	–	nA
I_5	positive MAC AGC		–	50	–	nA
I_5	negative MAC AGC		–	200	–	nA
Tuner AGC (note 15)						
	input voltage for tuner AGC starting point					
V_3	IF input = 200 µV; negative slope		3.0	3.5	–	V
V_3	IF input = 100 mV; negative slope		–	5.0	5.5	V
V_3	IF input = 200 µV; positive slope		7.0	7.5	–	V
V_3	IF input = 100 mV; positive slope		–	9.0	9.5	V
I_4	maximum current swing of tuner AGC output		3	5	–	mA
V_4	output saturation voltage	I_4 = 2 mA	–	–	300	mV
I_4	leakage current		–	–	1	µA
ΔV_i	input signal variation complete tuner control		0.5	2.0	4.0	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_3	minimum tuner take over voltage		–	–	1	V
Video switching circuit						
EXTERNAL VIDEO INPUT (AC coupled)						
$V_{10(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	–	1.0	–	V
I_{10}	input current		–	3.5	–	μA
V_{10}	top sync clamping level	I_{10} = 1 mA	–	3.3	–	V
INTERNAL VIDEO INPUT (DC coupled)						
$V_{12(p-p)}$	input signal voltage (peak-to-peak value)	V_O = 2 V(p-p)	–	2.0	–	V
$\|Z_{12}\|$	input impedance		–	2.0	–	kΩ
V_{12}	black level input voltage		–	3.3	–	V
VIDEO OUTPUT						
$V_{13(p-p)}$	output signal voltage (peak-to-peak value)		–	2.0	–	V
V_{13}	top sync level		–	2.7	–	V
V_{13}	noise clamping voltage level	I_{13} = 1 mA	–	2.5	–	V
I_{13}	internal bias current of npn emitter follower output transistor		–	1.5	–	mA
I_{13}	maximum source current		5	–	10	mA
B_{13}	bandwidth of output signal		–	5	–	MHz
	crosstalk of video signal	note 16				
α	external to internal		–	60	55	dB
α	internal to external		–	55	50	dB
VIDEO SWITCH INPUT (note 17)						
V_7	maximum voltage for external video signal		–	–	2	V
V_7	minimum voltage for internal video signal		1	–	–	V
I_7	minimum source current for internal video signal		–	–	300	μA
I_7	input current	V_7 = 0 V	–	–	–1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_7	input current	$V_7 = V_P$	–	–	3	µA
AFC circuit (note 18)						
AFC SAMPLE-AND-HOLD/SWITCH (note 19)						
	AFC switch:					
I_6	current level below which AFC outputs switches off		–	–	–500	µA
I_6	maximum AFC switch current	V_6 = 0 V	–	–	–1	mA
I_6	maximum leakage current		–	–	1	µA
AFC ANALOG OUTPUT ($V_9 > 8$ V; see Figs 4 and 5)						
$V_{8(p-p)}$	output voltage swing (peak-to-peak value)		10	–	11	V
I_8	maximum output current		500	–	–	µA
	control steepness		60	75	100	mV/kHz
V_8	AFC output voltage	AFC off	5	6	7	V
AFC DIGITAL OUTPUT (see Table 1)						
$V_{8,9}$	output voltage LOW		–	–	0.5	V
$V_{8,9}$	output voltage HIGH	50 kΩ load	4.5	–	5.5	V
Δf	frequency swing for switching AFC output Q1		65	80	100	kHz
$I_{8,9}$	maximum allowable output current		500	–	–	µA
AFC Analog SWITCH (note 20)						
I_9	minimum sink current for analog AFC		–	–	1.5	mA
V_9	minimum voltage for negative slope		–	–	10.2	V
V_9	minimum voltage for positive slope		–	–	8.0	V
V_9	maximum voltage for positive slope		10.2	–	–	V
I_9	output current	$V_9 = V_P$	–	500	–	µA
I_9	output current	V_9 = 8 to 10 V	–	150	–	µA
Video transmitter identification output (note 21)						
V_{18}	output voltage active	no sync; I_{18} = 1 mA	–	0.3	0.5	V
I_{18}	output current inactive	sync	–	–	3	µA
t_d	delay time of mute release after sync insertion		–	–	10	ms
I_{19}	allowed leakage current of identification detector capacitor		–	–	50	nA

Notes

1. All input signals are measured in RMS values at 100% carrier level and a frequency of 38.9 MHz.
2. On set AGC.
3. Input impedance selected so that a SAW filter can be applied without extra components.
4. Measured with 0 dB = 200 μV.
5. Measured at 10 mV(RMS) top sync input signal and the video output unloaded.
6. Projected zero point with internally switched demodulator.
7. With the AGC switch switched to ground, for the B/G standard, or with the identification capacitor switched to V_{CC} for the negative MAC standard.
8. With the AGC switch switched open for the L standard, or switched to V_{CC} for the positive MAC standard.
9. Measured in accordance with the test line given in Fig.8.
   - The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   - The differential phase is defined as the difference in degrees between the phase angle of the 4.4 MHz signal at 20% and 80% luminance signal.
10. Measured in accordance with the test line shown in Fig.9.

    The non-linearity is measured by comparing the differences between adjacent pairs of six luminance levels that make up the 5 step staircase. The measurement result is the largest percentage deviation in adjacent step values. The sign is always positive.
11. Measured with a 75 Ω source: $S/N = 20 \log \frac{V_o \text{ black-to white}}{V_n \text{ (RMS) at B = 5 MHz}}$
12. The internal circuit of pin 20 behaves as an internal voltage source of 4.5 V with an input resistance of 15 kΩ. Using the system switch three conditions can be obtained:

    Negative modulation with top sync level AGC. This is achieved with pin 20 connected to ground.

    Positive modulation with white level AGC. This is achieved with pin 20 open, or connected to 5 V.

    Positive modulation with top white AGC and an increased time constant for MAC signals. This is achieved with pin 20 connected to V_{CC}.
13. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 200 μV to 80 mV input signals.
14. Measured with a capacitor of 2.2 μF connected to pin 5. A step is made from 80 mV to 200 μV input signals.
15. It is possible to adjust the tuner AGC over the whole AGC range of the IF amplifier for both pnp and npn tuners. Tuner AGC starting point is defined as an output current of 0.2 mA for pnp and 1.8 mA for npn, in an application with a resistance of 6 kΩ to V_P at pin 4.
16. Crosstalk is defined as: $20 \log \frac{V_o \text{unwanted video black-to-white}}{V_o \text{wanted video black-to-white}}$ measured at 4.4 MHz
17. The video switch is controlled by a voltage on pin 7. The switching level is approximately 1.4 V. With pin 7 open-circuit internal video is selected; with pin 7 pulled to ground external video is selected.
18. Measurement taken with an input 10 mV(RMS). The unloaded Q factor of the reference tuned circuit is 70.
19. Switching off the AFC is obtained by a voltage of less than 2 V on pin 6. Normally this is achieved by pulling pin 6 to ground.
20. Switching to the normal analog AFC mode can be done by pulling pin 9 to a voltage above 10.2 V. Normally this is achieved by pulling pin 9 to V_P.
    The inverse analog AFC mode can only be obtained by a voltage of between 8 and 10 V applied to pin 9.

21. All timing figures defined with a capacitor of 2.2 nF at pin 19. The identification can be speeded up by lowering the value of this capacitor, however this makes the circuit also less sensitive if the video signal is disturbed (airplane flutter etc.). If the identification is only used as a sound mute a capacitor of 47 nF is recommended to improve the sensitivity.

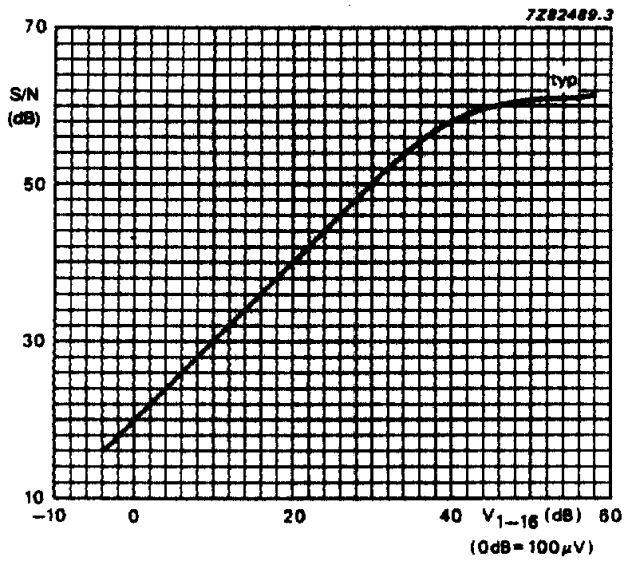


Fig.2 Signal-to-noise ratio as a function of video input.

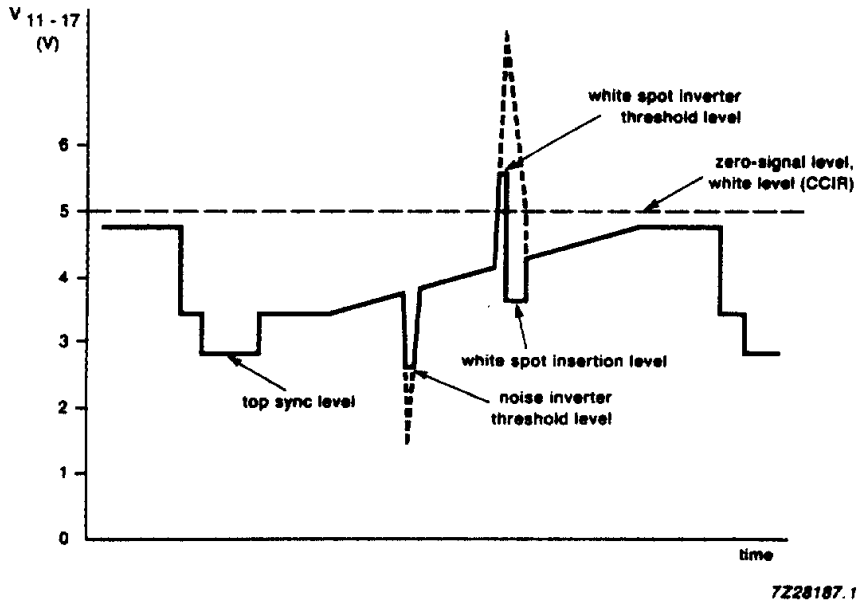


Fig.3 Video waveform showing white spot threshold and insertion levels, and noise clamping levels

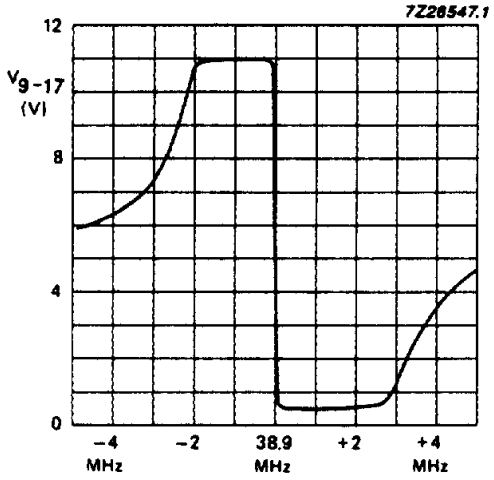


Fig.4 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

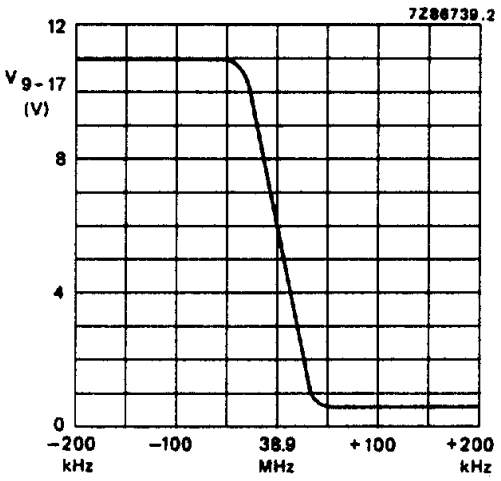
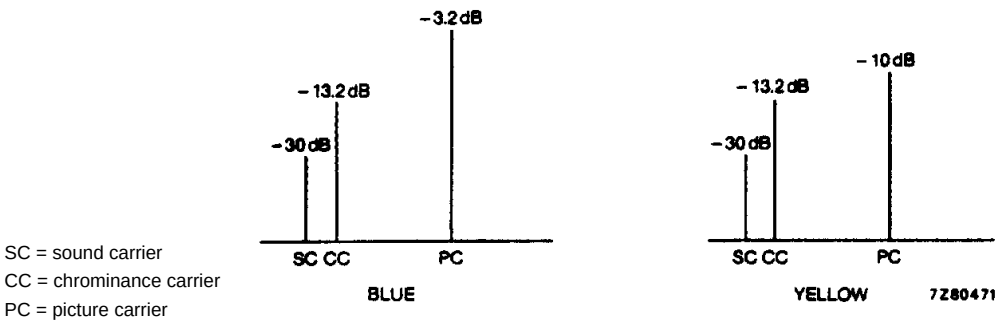


Fig.5 Analog AFC output voltage as a function of frequency pin 9 above 10 V.

Table 1 Digital AFC truth table

INPUT FREQUENCY	Q1	Q2
> IF +40 kHz	0	1
> IF	1	1
< IF	1	0
< IF –40 kHz	0	0



SC = sound carrier
CC = chrominance carrier
PC = picture carrier

all with respect to top sync level

Fig.6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

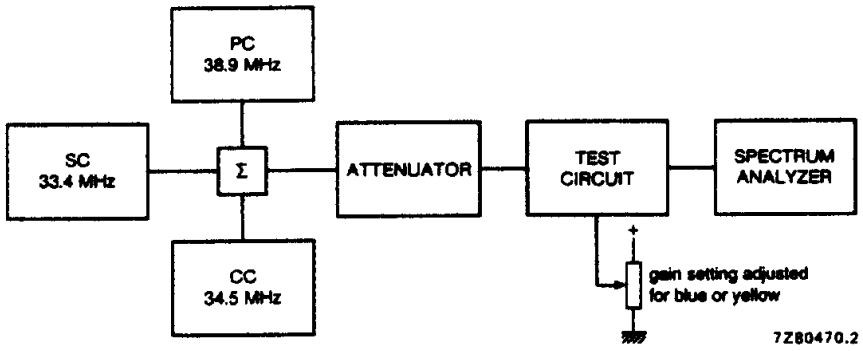


Fig.7 Test set-up intermodulation measurements.

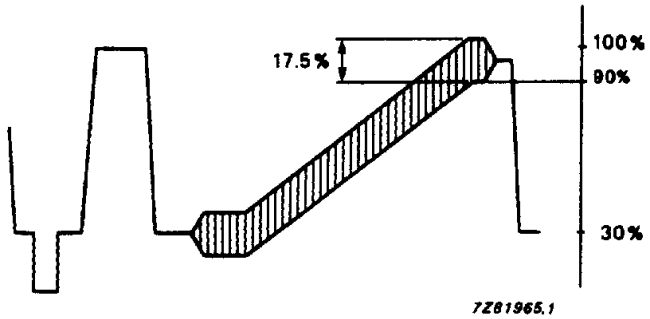


Fig.8 Video output signal.

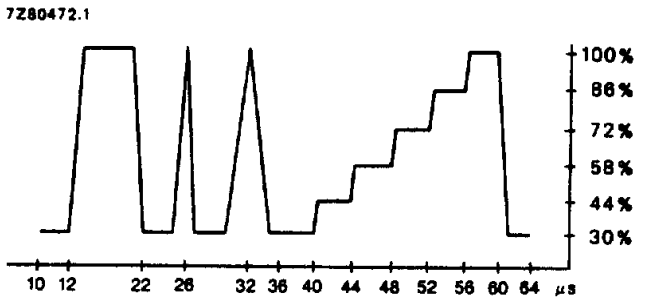
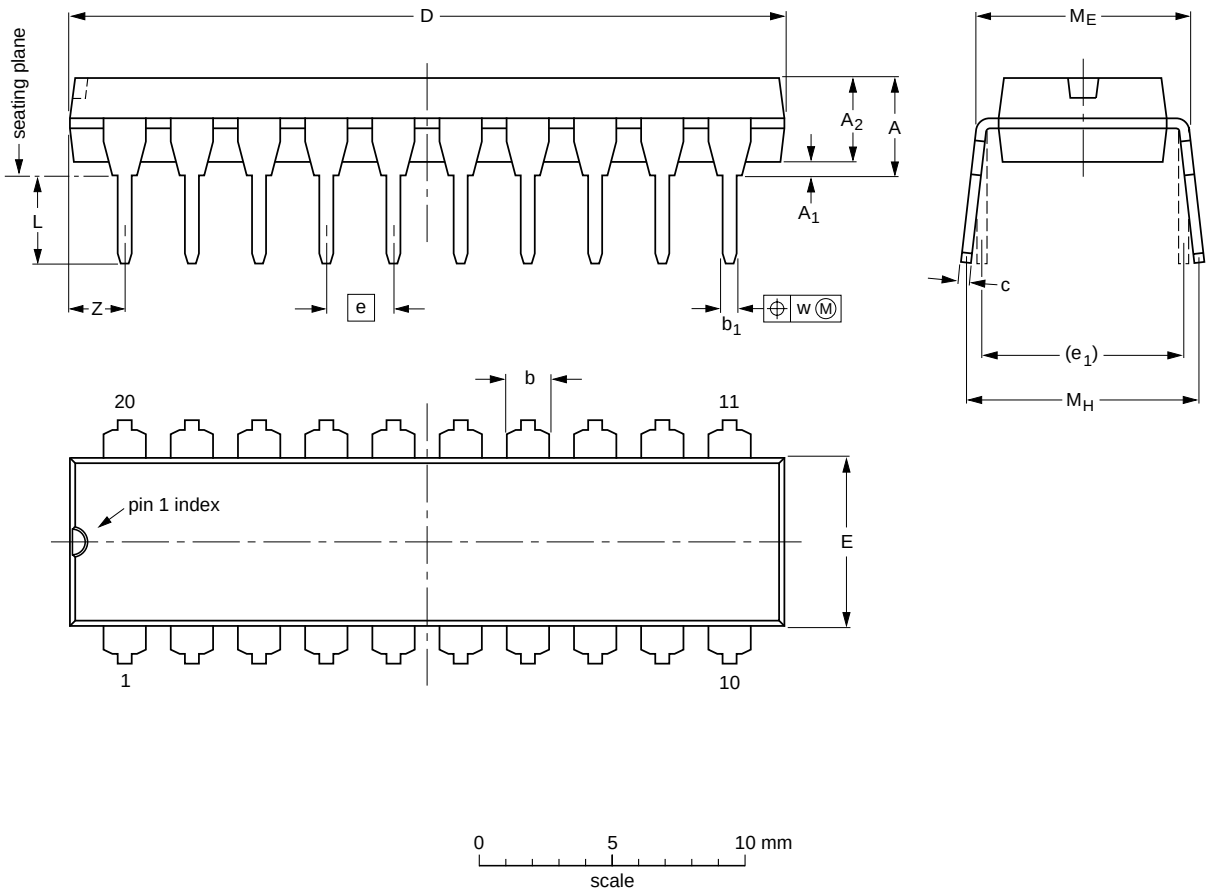


Fig.9 E.B.U. test signal wave form (line 330).

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.