

TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- Low Noise
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$ Typ at $f = 1 \text{ kHz}$
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description/ordering information

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

description/ordering information (continued)

ORDERING INFORMATION

TA	V _{IO} max AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074CN	TL074CN
		SOIC (D)	Tube of 75	TL071CD	TL071C
			Reel of 2500	TL071CDR	
			Tube of 75	TL072CD	TL072C
			Reel of 2500	TL072CDR	
			Tube of 50	TL074CD	TL074C
			Reel of 2500	TL074CDR	
		SOP (NS)	Reel of 2000	TL074CNSR	TL074
		SOP (PS)	Reel of 2000	TL071CPSR	TL071
			Reel of 2000	TL072CPSR	T072
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072
			Tube of 90	TL074CPW	T074
			Reel of 2000	TL074CPWR	
	6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074ACN	TL074ACN
		SOIC (D)	Tube of 75	TL071ACD	071AC
			Reel of 2500	TL071ACDR	
			Tube of 75	TL072ACD	072AC
			Reel of 2500	TL072ACDR	
			Tube of 50	TL074ACD	TL074AC
			Reel of 2500	TL074ACDR	
		SOP (PS)	Reel of 2000	TL072ACPSR	T072A
	SOP (NS)	Reel of 2000	TL074ACNSR	TL074A	
	3 mV	PDIP (P)	Tube of 50	TL071BCP	TL071BCP
			Tube of 50	TL072BCP	TL072BCP
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN
		SOIC (D)	Tube of 75	TL071BCD	071BC
Reel of 2500			TL071BCDR		
Tube of 75			TL072BCD	072BC	
Reel of 2500			TL072BCDR		
Tube of 50			TL074BCD	TL074BC	
Reel of 2500			TL074BCDR		
SOP (NS)		Reel of 2000	TL074BCNSR	TL074B	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



**TL071, TL071A, TL071B, TL072
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LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

description/ordering information (continued)

ORDERING INFORMATION

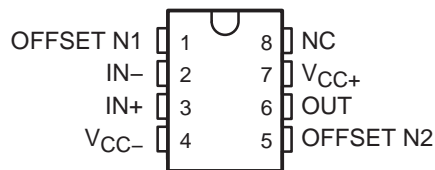
TA	V _{IOMax} AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
		-55°C to 125°C	6 mV	CDIP (JG)	Tube of 50
CFP (U)	Tube of 150			TL072MU	TL072MU
LCCC (FK)	Tube of 55			TL072MFK	TL072MFK
9 mV	CDIP (J)		Tube of 25	TL074MJ	TL074MJ
	CFP (W)		Tube of 25	TL074MW	TL074MW
	LCCC (FK)		Tube of 55	TL074MFK	TL074MFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

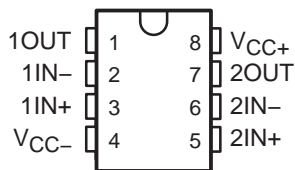
TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

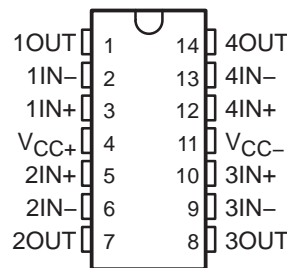
TL071, TL071A, TL071B
D, P, OR PS PACKAGE
(TOP VIEW)



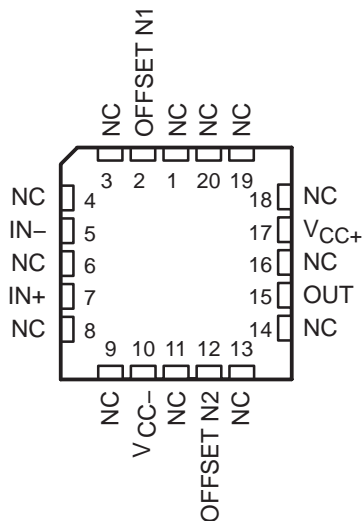
TL072, TL072A, TL072B
D, JG, P, PS, PW, OR U PACKAGE
(TOP VIEW)



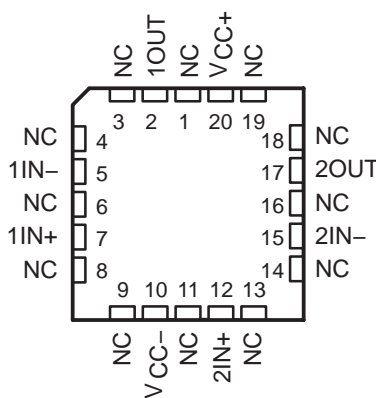
TL074A, TL074B
D, J, N, NS, OR PW PACKAGE
TL074 . . . D, J, N, NS, PW,
OR W PACKAGE
(TOP VIEW)



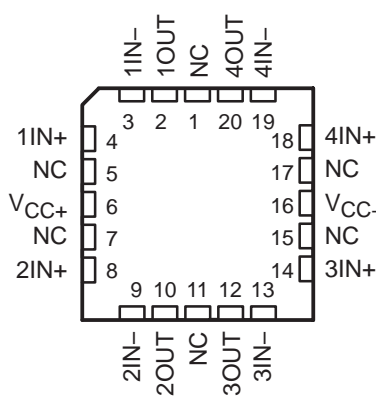
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)

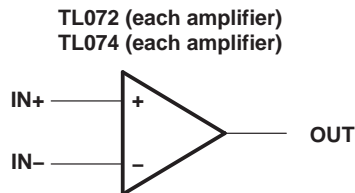
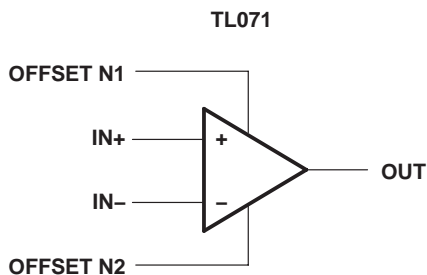


TL074
FK PACKAGE
(TOP VIEW)



NC – No internal connection

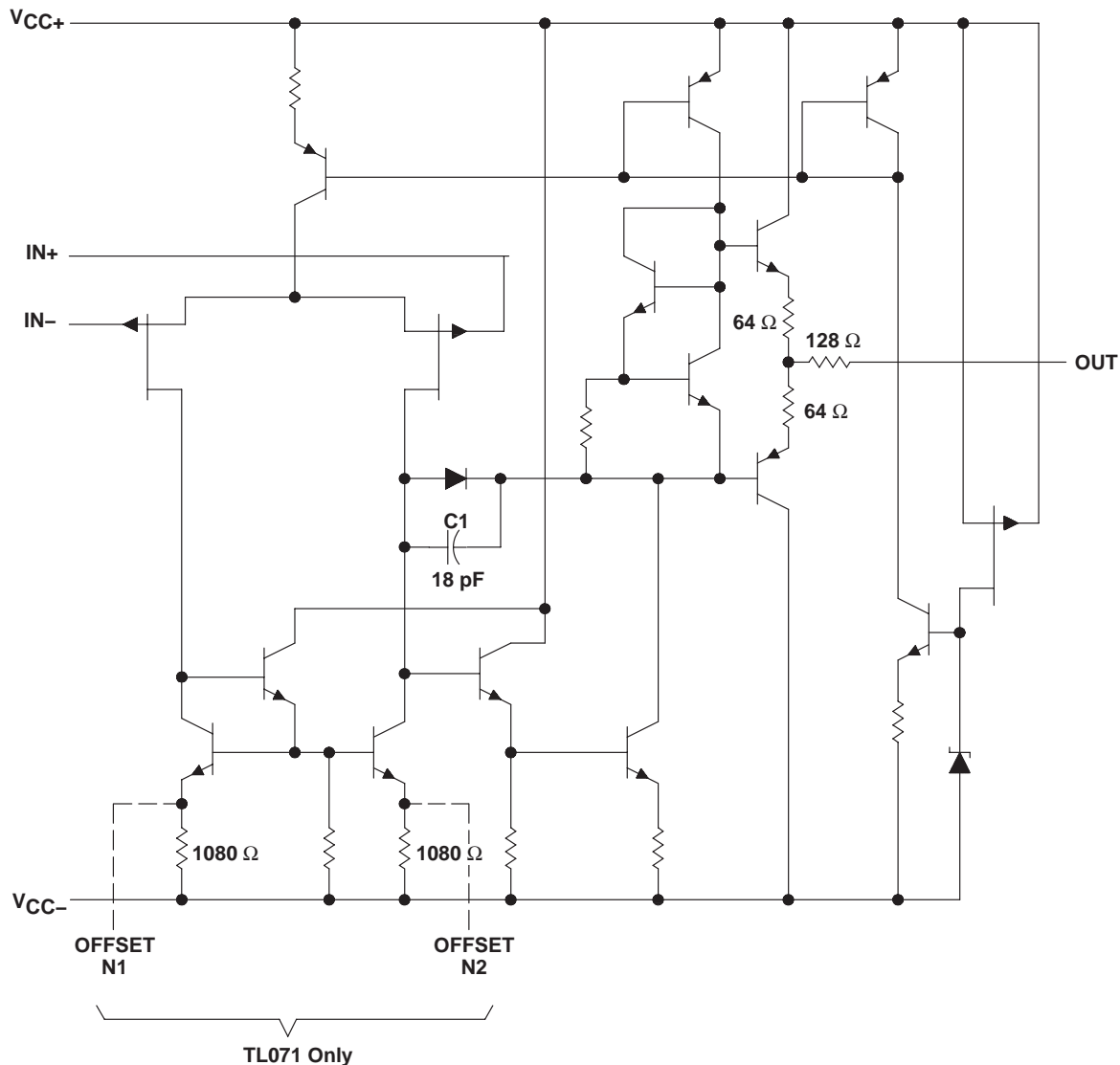
symbols



TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+}	18 V
V_{CC-}	-18 V
Differential input voltage, V_{ID} (see Note 2)	± 30 V
Input voltage, V_I (see Notes 1 and 3)	± 15 V
Duration of output short circuit (see Note 4)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package (8 pin)	97°C/W
D package (14 pin)	86°C/W
N package	80°C/W
NS package	76°C/W
P package	85°C/W
PS package	95°C/W
PW package (8 pin)	149°C/W
PW package (14 pin)	113°C/W
U package	185°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8): FK package	5.61°C/W
J package	15.05°C/W
JG package	14.5°C/W
W package	14.65°C/W
Operating virtual junction temperature, T_J	150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds:	
D, N, NS, P, PS, or PW package	260°C
J, JG, or W package	300°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 6. The package thermal impedance is calculated in accordance with JESD 51-7.
 7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 8. The package thermal impedance is calculated in accordance with MIL-STD-883.



**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T _A ‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	V _O = 0, R _S = 50 Ω	25°C Full range	3	10	13	3	3	6	2	2	3	3	3	6	mV
αV _{IO}	V _O = 0, R _S = 50 Ω	Full range	18			18			18			18			μV/°C
I _{IO}	V _O = 0	25°C Full range	5	100	10	5	100	2	5	100	2	5	100	pA	
I _{IB}	V _O = 0	25°C Full range	65	200	7	65	200	7	65	200	65	200	20	nA	
V _{ICR}	Common-mode input voltage range	25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15	±11	-12 to 15		V	
V _{OM}	Maximum peak output voltage	25°C	±12	±13.5		±12	±13.5		±12	±13.5	±12	±13.5		V	
	output voltage swing	Full range	±12			±12			±12		±12				
			±10			±10			±10		±10				
A _{VD}	Large-signal differential voltage amplification	25°C Full range	25	200	15	50	200	25	50	200	50	200	25	V/mV	
B ₁	Unity-gain bandwidth	25°C	3			3			3		3			MHz	
r _i	Input resistance	25°C	10 ¹²			10 ¹²			10 ¹²		10 ¹²			Ω	
CMRR	Common-mode rejection ratio	25°C	70	100		75	100		75	100	75	100		dB	
kSVR	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	25°C	70	100		80	100		80	100	80	100		dB	
I _{CC}	Supply current (each amplifier)	25°C	1.4	2.5		1.4	2.5		1.4	2.5	1.4	2.5		mA	
V _{O1} /V _{O2}	Crosstalk attenuation	25°C	120			120			120		120			dB	

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

‡ Full range is T_A = 0°C to 70°C for TL07_C, TL07_AC, TL07_BC and is T_A = -40°C to 85°C for TL07_I.

§ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.



TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_A ‡	TL071M TL072M			TL074M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C	3	6		3	9	mV	
		Full range			9		15		
αV_{IO} Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range	18			18			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current	$V_O = 0$	25°C	5	100		5	100	pA	
		Full range	20			20			nA
I_{IB} Input bias current‡	$V_O = 0$	25°C	65	200		65	200	pA	
		Full range	50			50			nA
V_{ICR} Common-mode input voltage range		25°C	± 11	-12 to 15		± 11	-12 to 15	V	
V_{OM} Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	± 12	± 13.5		± 12	± 13.5	V	
	$R_L \geq 10\ \text{k}\Omega$	Full range	± 12			± 12			
	$R_L \geq 2\ \text{k}\Omega$		± 10			± 10			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	35	200		35	200	V/mV	
		Full range	15			15			
B_1 Unity-gain bandwidth	$T_A = 25^\circ\text{C}$		3			3			MHz
r_i Input resistance	$T_A = 25^\circ\text{C}$		10^{12}			10^{12}			Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
I_{CC} Supply current (each amplifier)	$V_O = 0, \text{ No load}$	25°C	1.4	2.5		1.4	2.5	mA	
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C	120			120			dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is $T_A = -55^\circ\text{C to } 125^\circ\text{C}$.

**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL07xM			ALL OTHERS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_I = 10\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figure 1	5	13		8	13		$\text{V}/\mu\text{s}$
t_r	Rise-time overshoot factor $V_I = 20\text{ mV}$, $C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Figure 1	0.1			0.1			μs
		20%			20%			
V_n	Equivalent input noise voltage $R_S = 20\ \Omega$	$f = 1\text{ kHz}$			18			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to }10\text{ kHz}$			4			μV
I_n	Equivalent input noise current $R_S = 20\ \Omega$, $f = 1\text{ kHz}$	0.01			0.01			$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion $V_{I\text{rms}} = 6\text{ V}$, $R_L \geq 2\text{ k}\Omega$, $f = 1\text{ kHz}$ $A_{VD} = 1$, $R_S \leq 1\text{ k}\Omega$	0.003%			0.003%			

PARAMETER MEASUREMENT INFORMATION

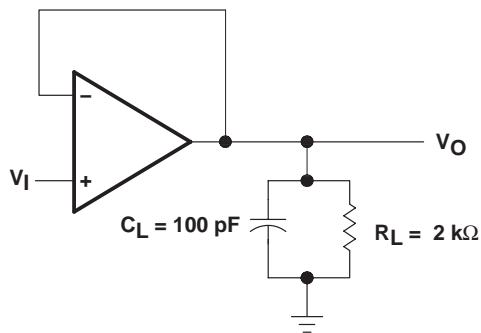


Figure 1. Unity-Gain Amplifier

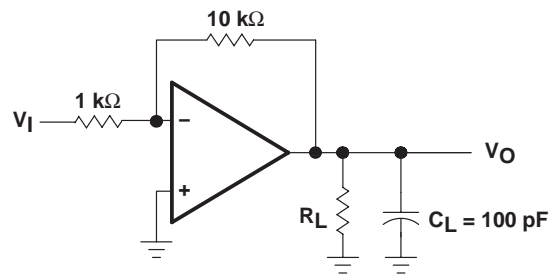


Figure 2. Gain-of-10 Inverting Amplifier

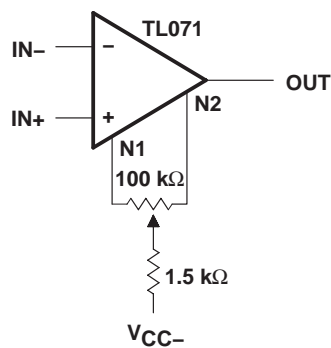


Figure 3. Input Offset-Voltage Null Circuit

TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency	5, 6, 7
		vs Free-air temperature	8
		vs Load resistance	9
		vs Supply voltage	10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature	11
		vs Frequency	12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
$CMRR$	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
P_D	Total power dissipation	vs Free-air temperature	17
		Normalized slew rate	vs Free-air temperature
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
		Large-signal pulse response	vs Time
V_O	Output voltage	vs Elapsed time	22



**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B**
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS†

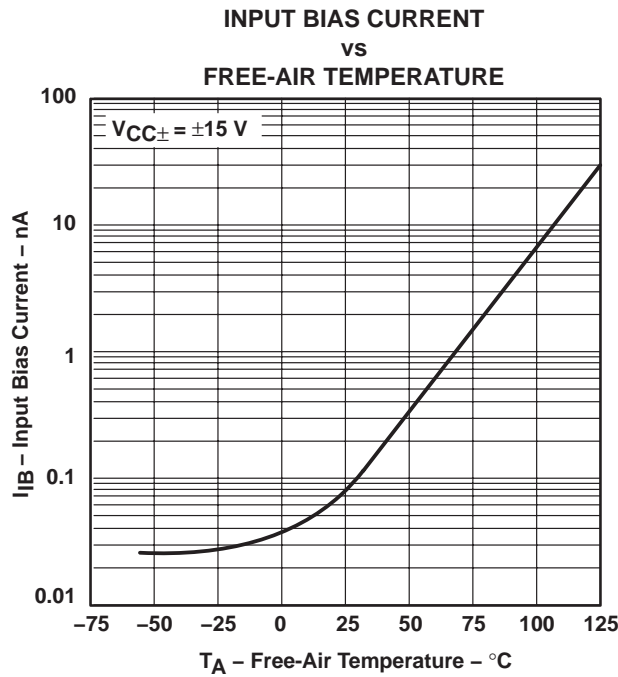


Figure 4

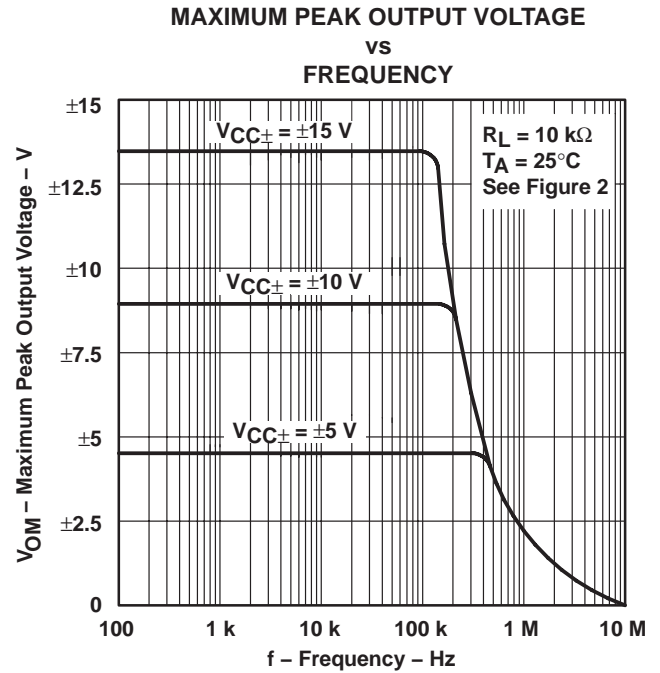


Figure 5

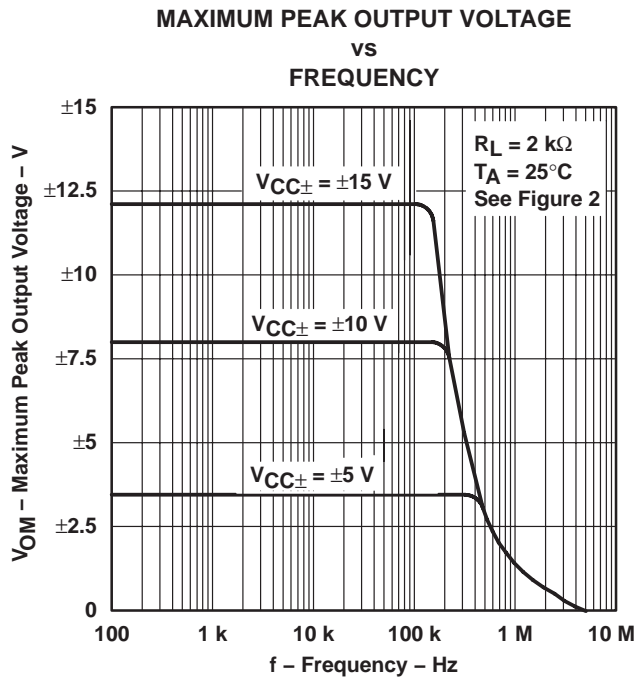


Figure 6

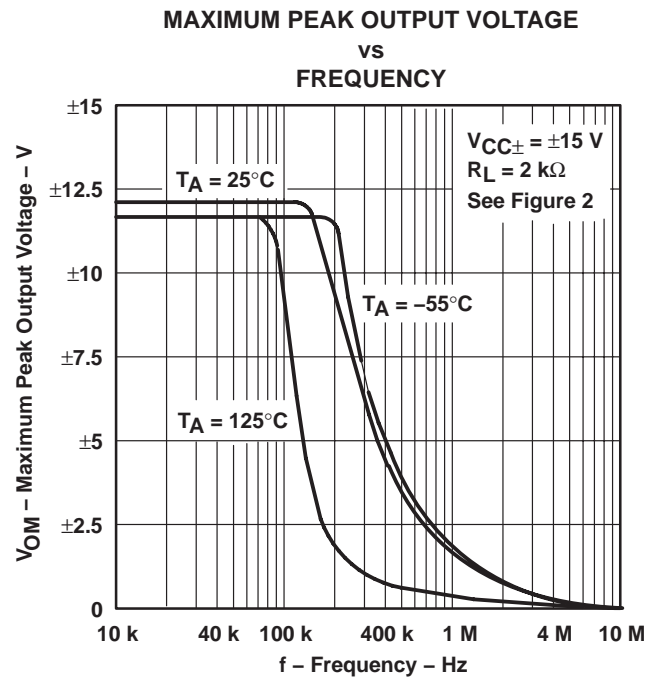


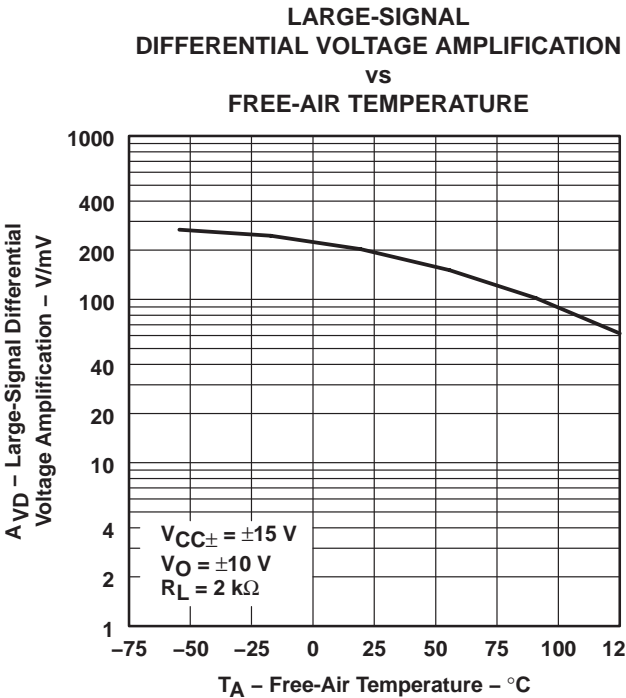
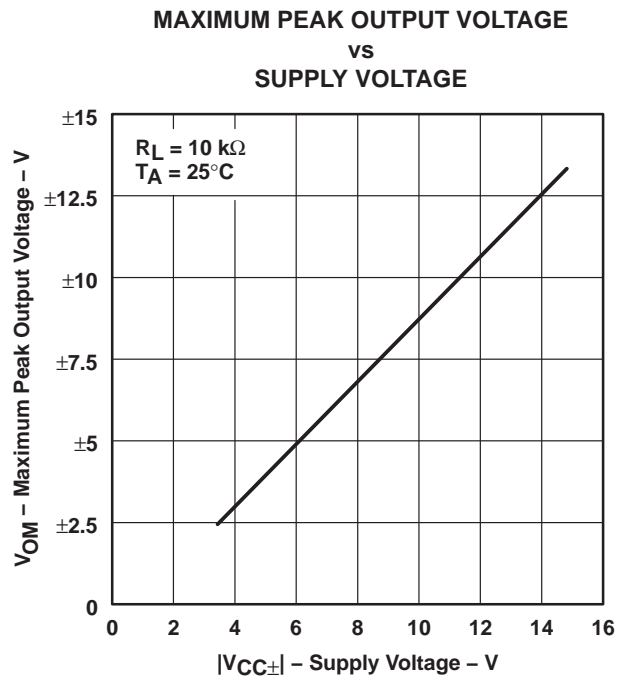
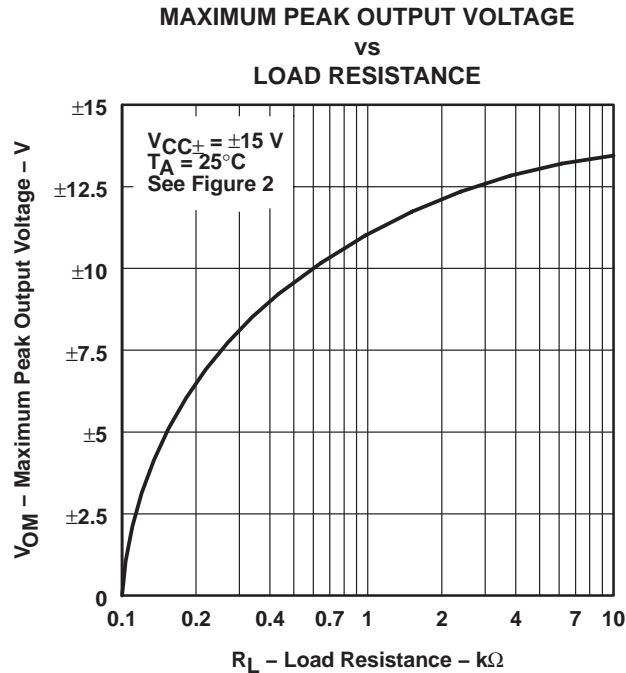
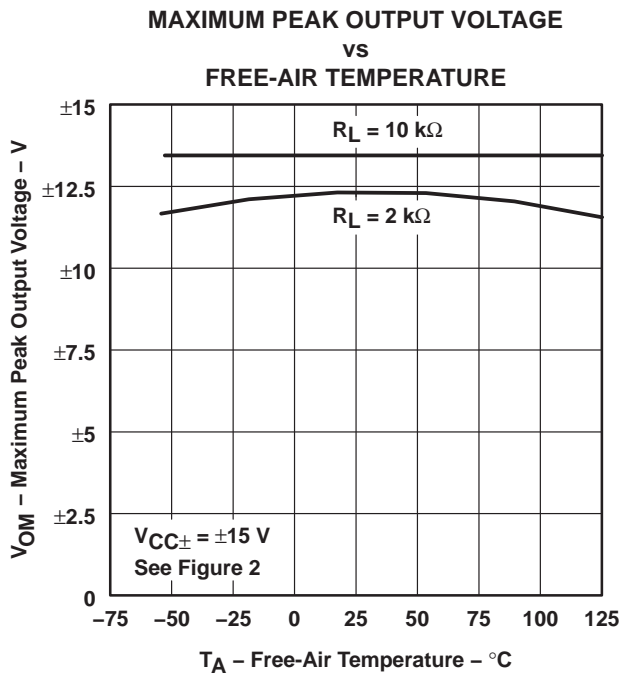
Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 AND PHASE SHIFT
 vs
 FREQUENCY

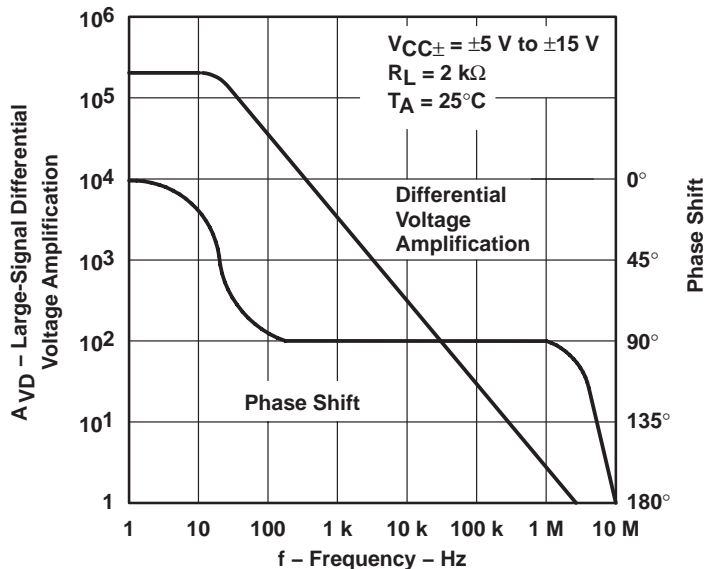


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH
 AND PHASE SHIFT
 vs
 FREE-AIR TEMPERATURE

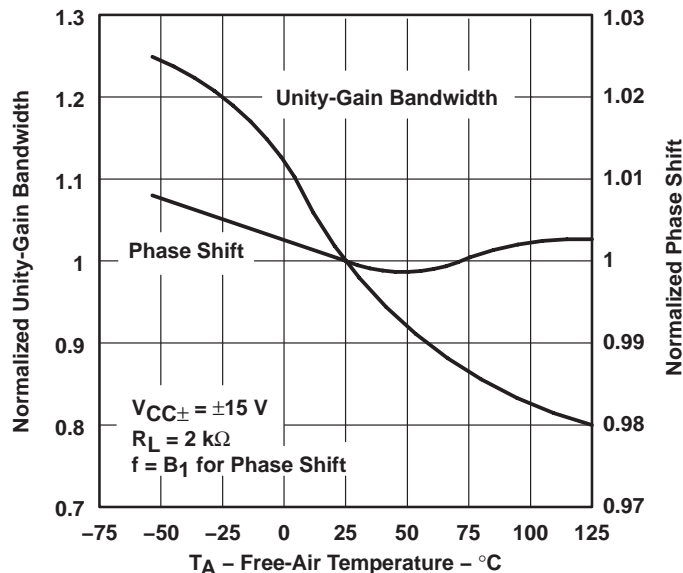


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

TYPICAL CHARACTERISTICS†

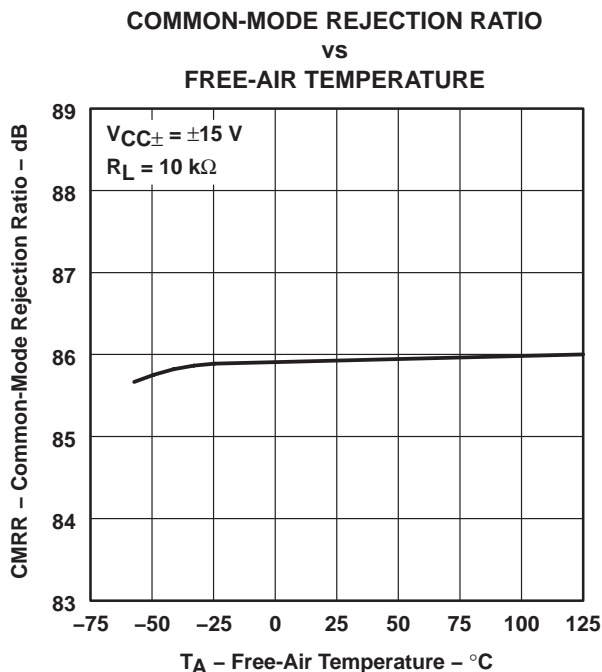


Figure 14

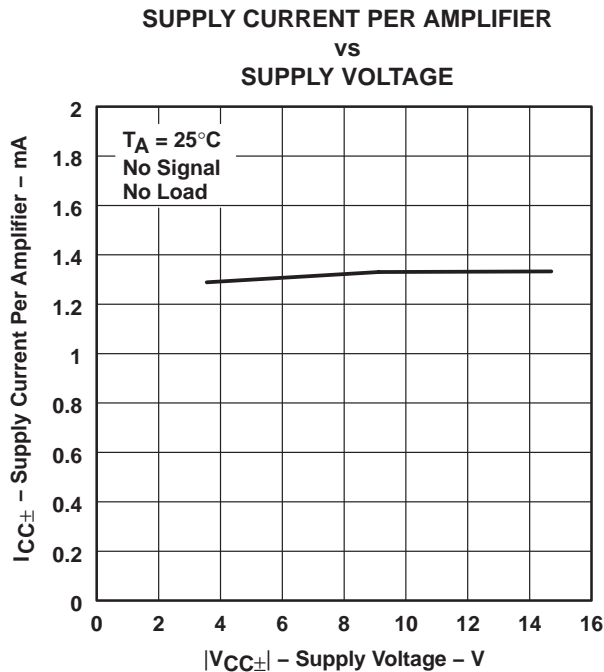


Figure 15

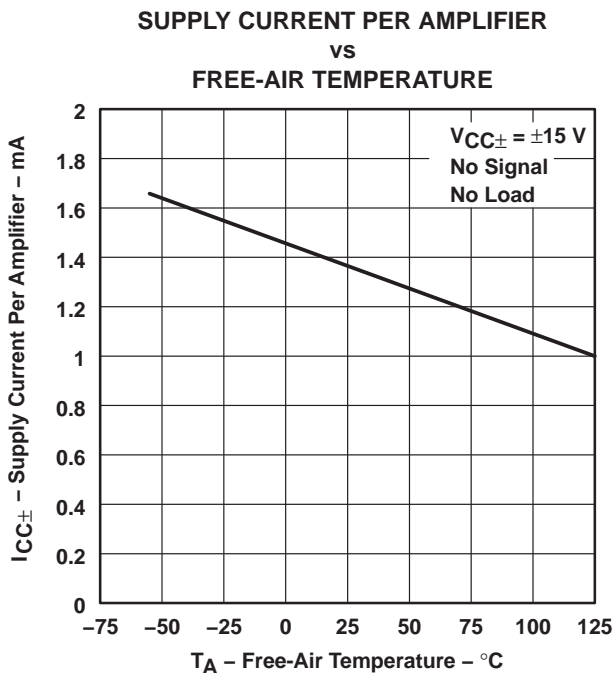


Figure 16

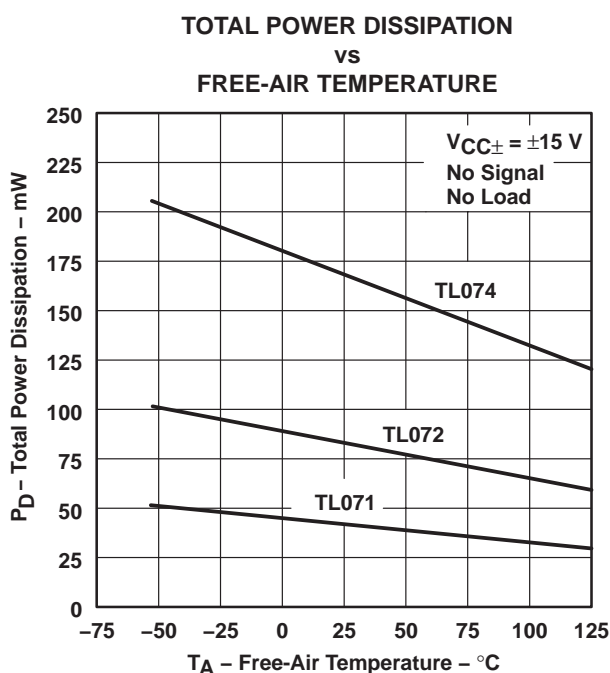


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

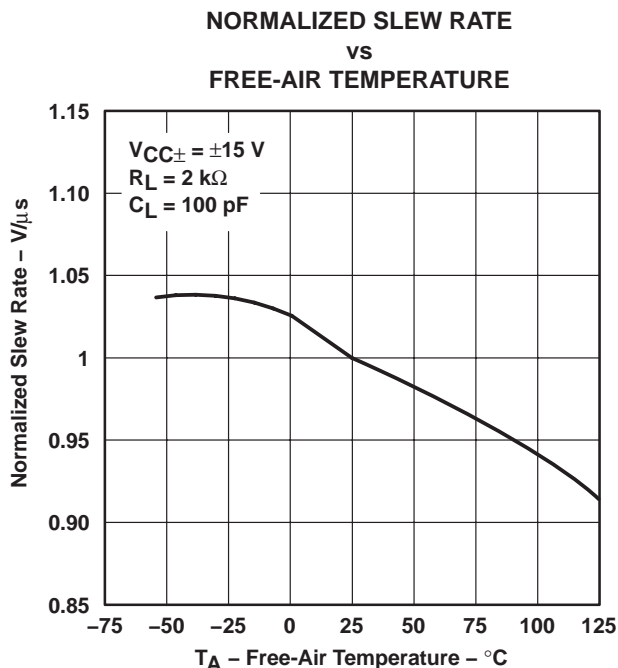


Figure 18

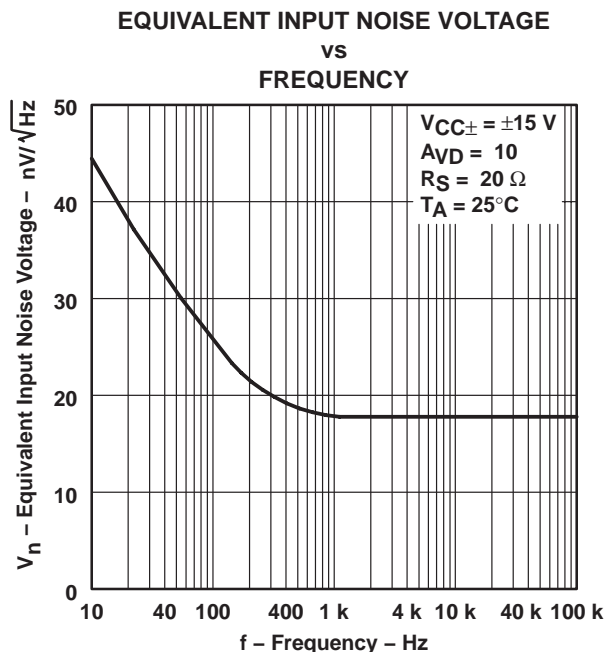


Figure 19

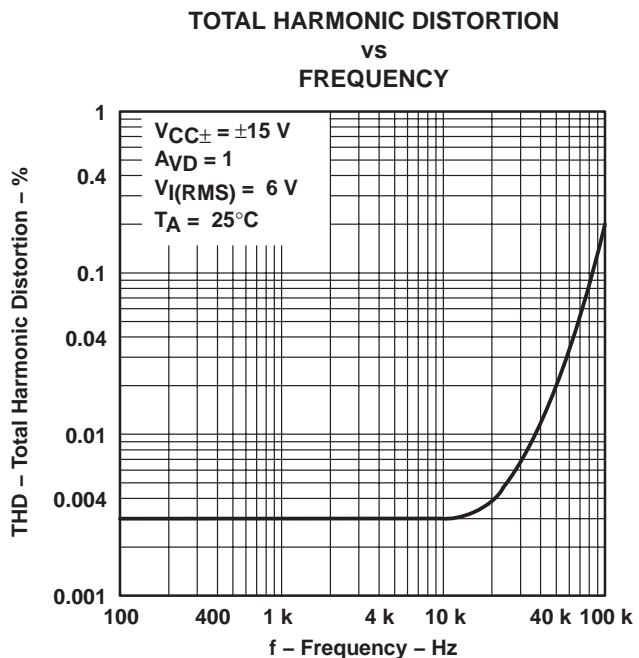


Figure 20

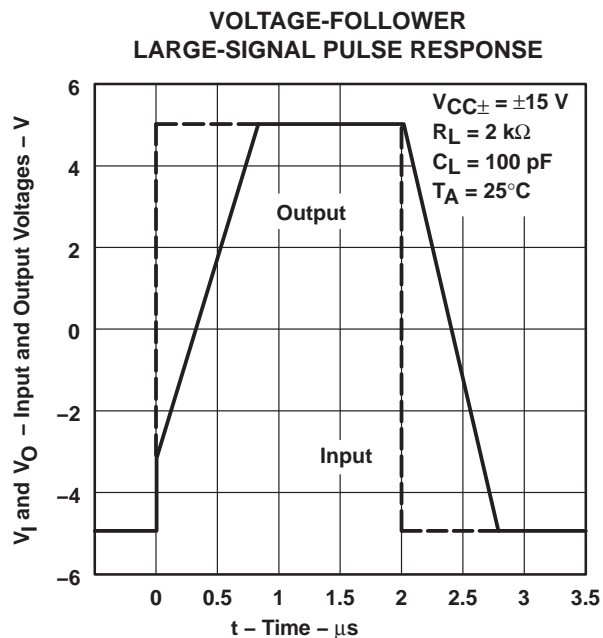


Figure 21

TYPICAL CHARACTERISTICS

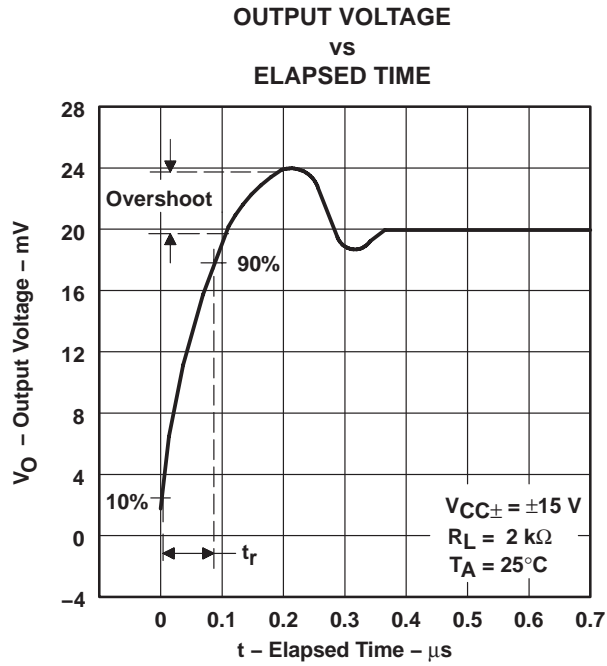


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

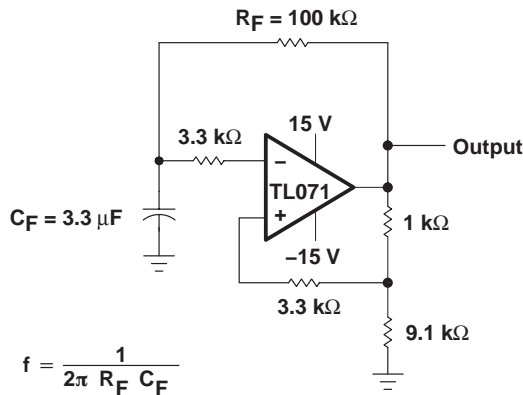


Figure 23. 0.5-Hz Square-Wave Oscillator

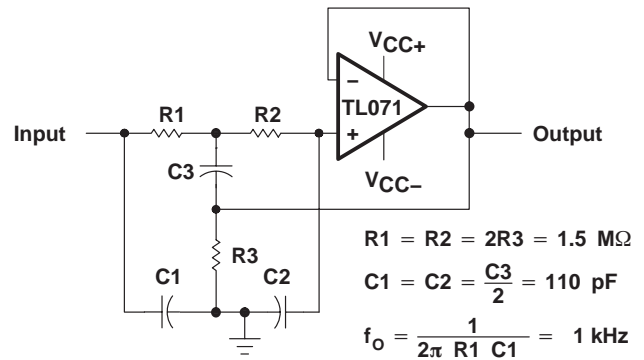


Figure 24. High-Q Notch Filter

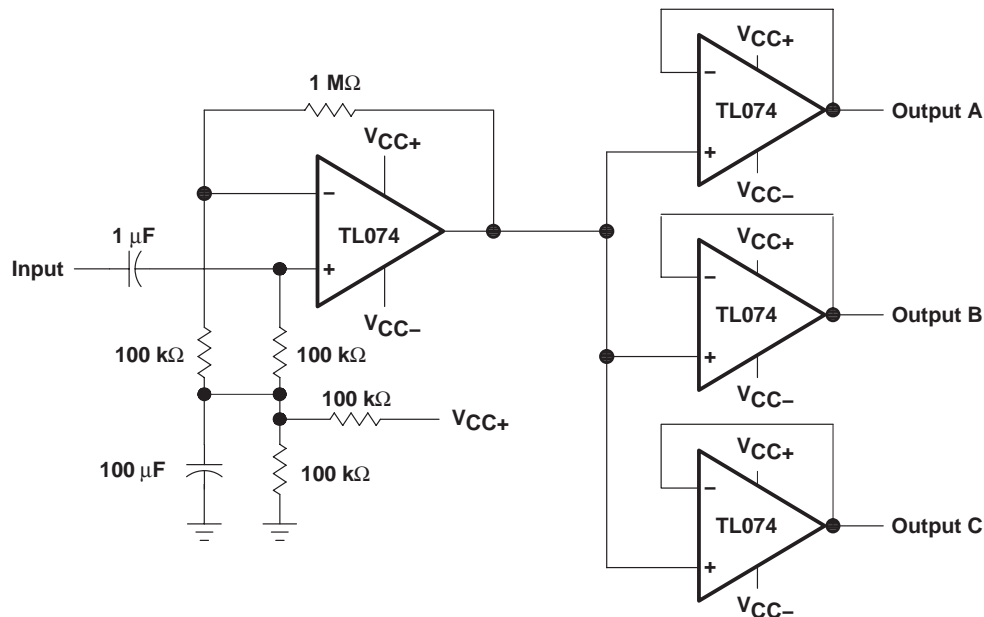
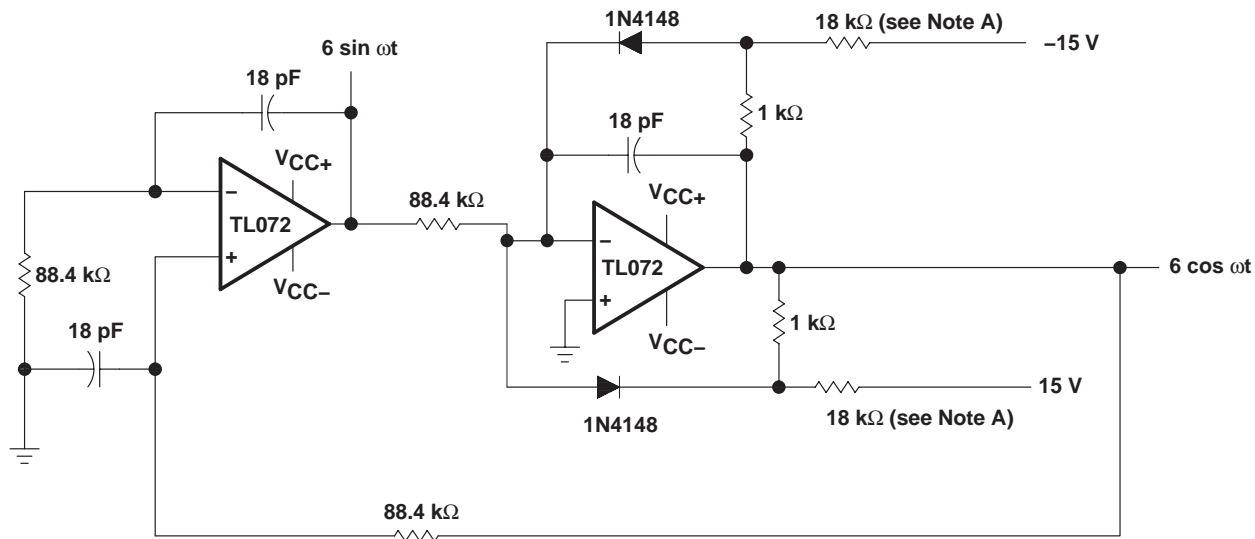


Figure 25. Audio-Distribution Amplifier

TL071, TL071A, TL071B, TL072
TL072A, TL072B, TL074, TL074A, TL074B
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS080G – SEPTEMBER 1978 – REVISED SEPTEMBER 2003

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

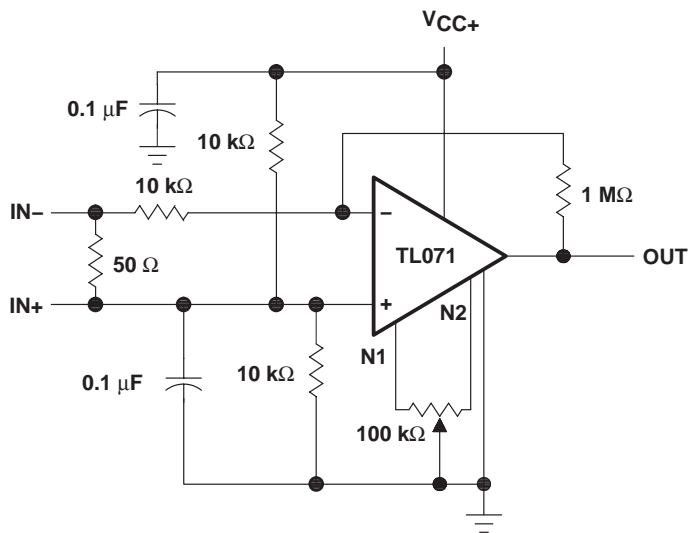


Figure 27. AC Amplifier

JG (R-GDIP-T8)

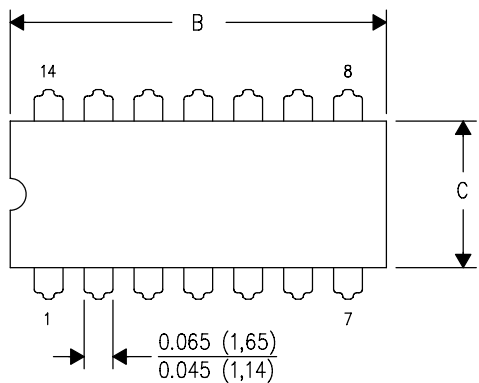
CERAMIC DUAL-IN-LINE



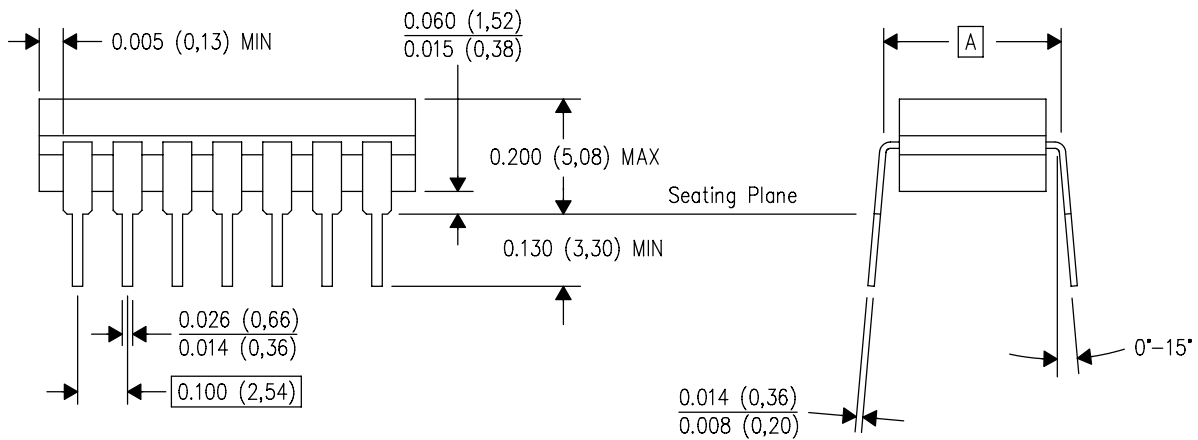
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**)
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

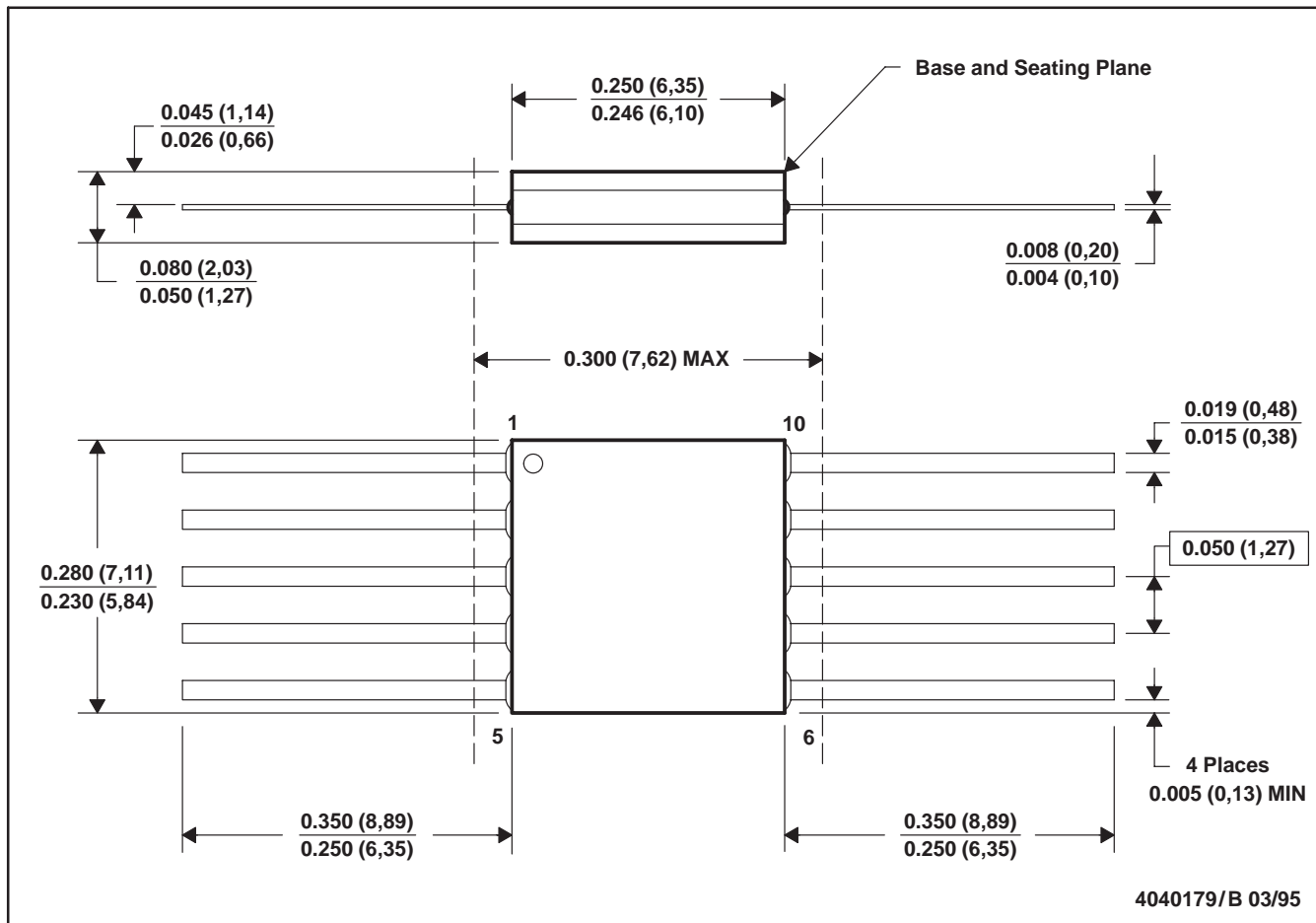


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

U (S-GDFP-F10)

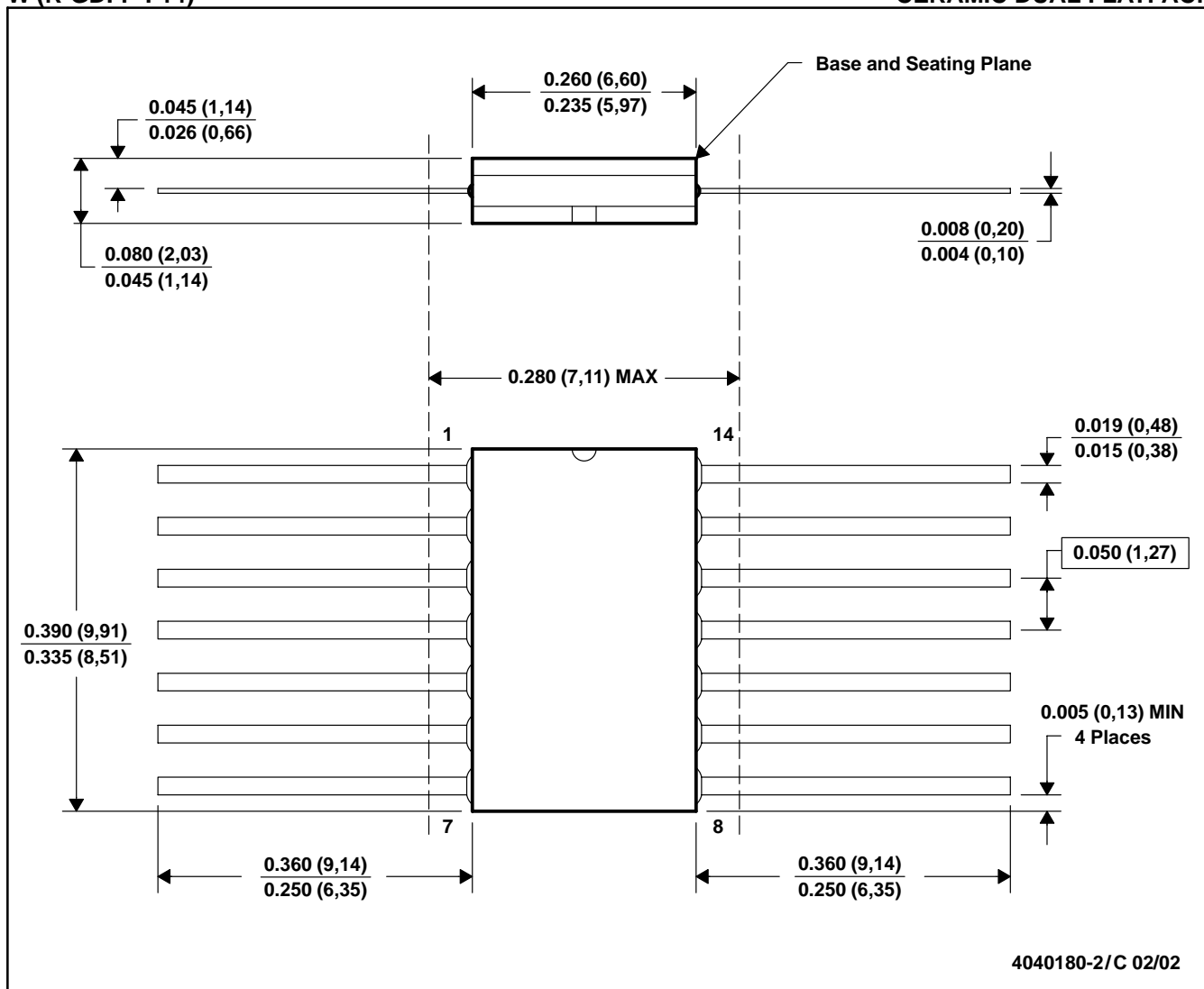
CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



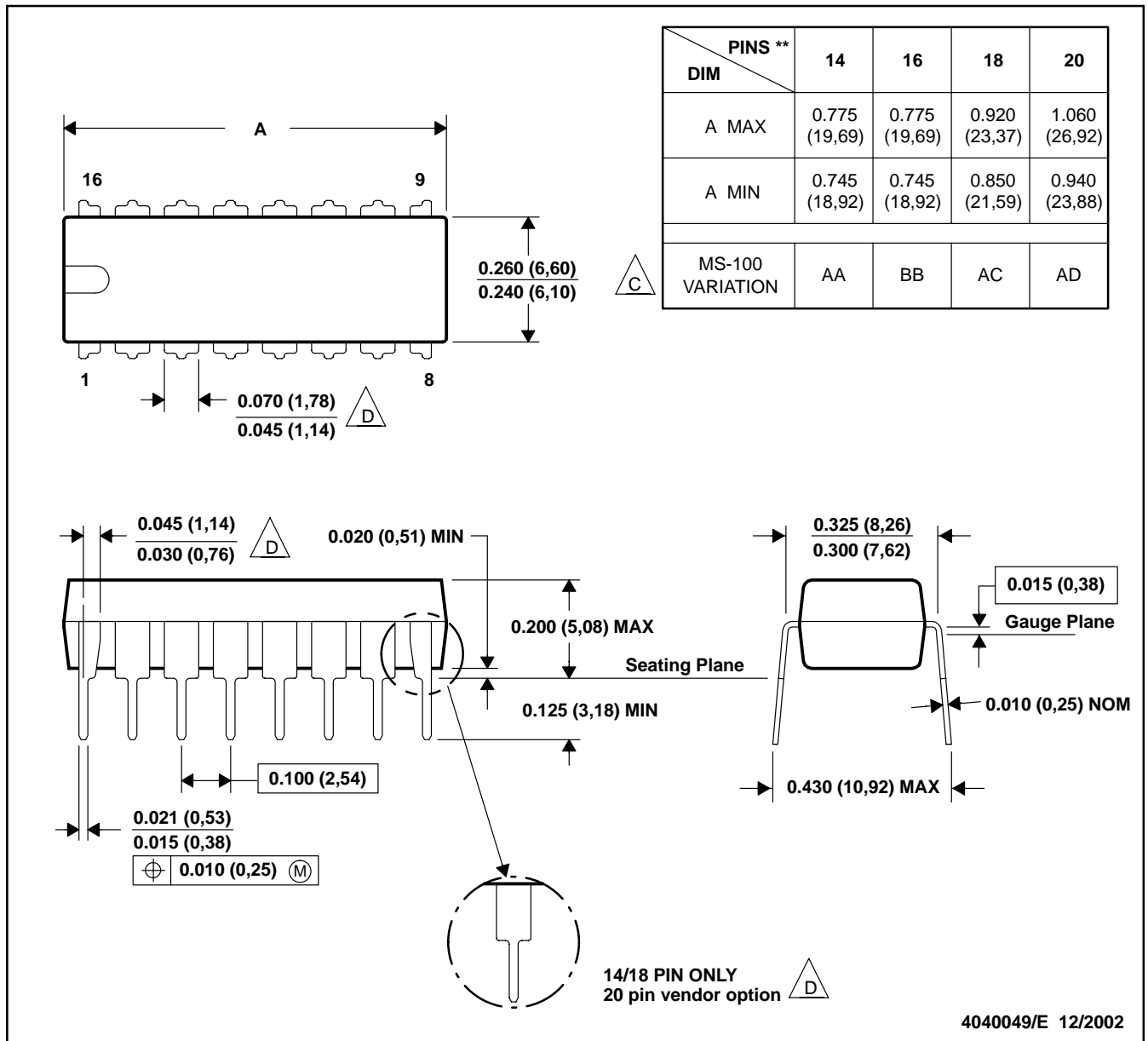
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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