



SANYO Semiconductors

DATA SHEET

LA4525

Monolithic Linear IC

For Radio Cassette Recorders

Dual AF Power Amplifier

Overview

The LA4525 requires only a small number of external components to drive either two 4Ω speakers or one 8Ω speaker. The output power is typically 0.65W when driving two 4Ω speakers.

Features

- Two-channel (dual) or single-channel (BTL) operation
- Requires only a few external components
- 0.65W (typ) output power into two 4Ω speakers
- Wide power supply range : 3 to 15V
- 8-pin DIP (No heat sink needed)

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$	$R_g = 0$	15	V
Allowable power dissipation	$P_d\ max$	Note	1.5	W
Operating temperature	T_{opr}		-25 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +150	$^\circ\text{C}$

Note : Mounted on a 50×50×1.6mm³ heat dissipating board

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		6	V
Load resistance range	R_L		4	Ω
Supply voltage range	$V_{CC\ op}$	Not in excess of package P_d	3 to 15	V

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SANYO Semiconductor Co., Ltd.

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LA4525

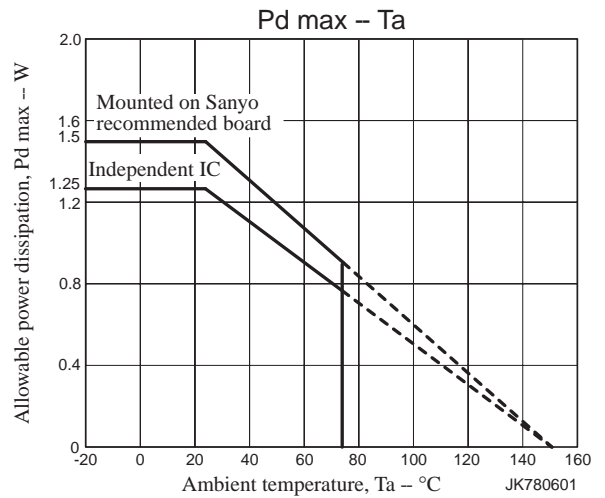
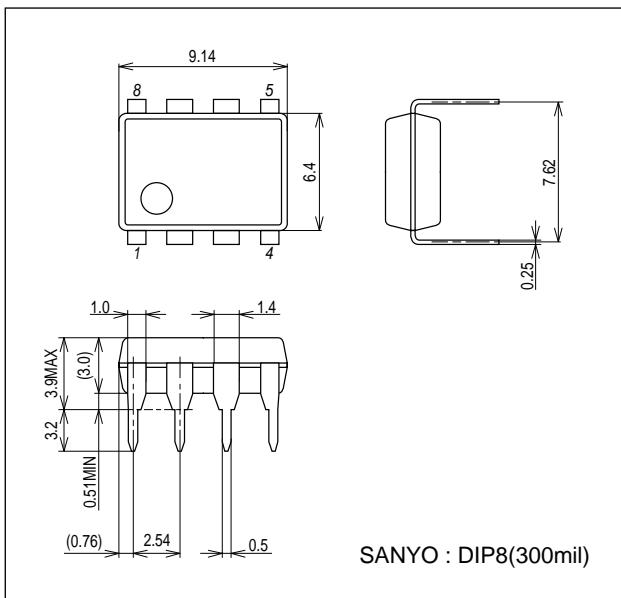
Electrical Characteristics at $V_{CC} = 6V$, $T_a = 25^\circ C$, $R_L = 4\Omega$, $f = 1kHz$, $R_g = 600\Omega$,
Dual operation unless otherwise noted

Parameter	Symbol	Condition	min	typ	max	Unit
Quiescent supply current	I_{CCO}	$R_g = 0\Omega$	10	15	30	mA
Output power	P_{O1}	THD = 10%	0.45	0.65		W
	P_{O2}	$V_{CC} = 9V$, $R_L = 8\Omega$, THD = 10%		1.0		W
Voltage gain	VG	$V_O = 0dBm$	38	40	42	dB
Total harmonic distortion	THD	$P_O = 0.1W$		0.2	0.7	%
Output noise voltage	V_{NO}	$R_g = 0\Omega$, DIN AUDIO filter		100	400	μV
Supply voltage ripple rejection	SVRR	$R_g = 0\Omega$, $f_R = 100Hz$, $V_R = 0dBm$	35	43		dB
Channel separation	CH Sep	$V_O = 0dBm$, $R_g = 0\Omega$	45	55		dB
Input resistance	R_i		70	100	130	k Ω

Package Dimensions

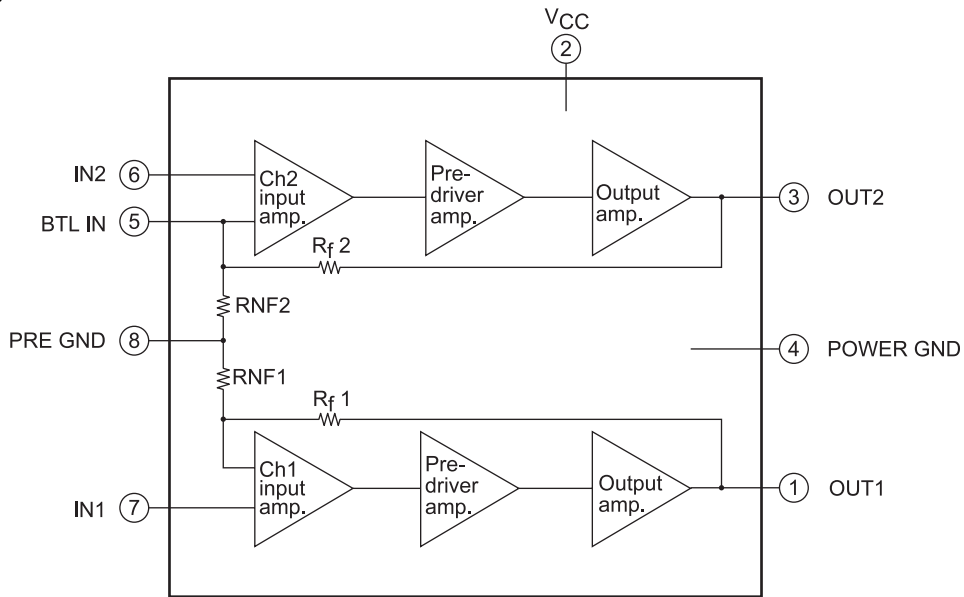
unit : mm (typ)

3001D

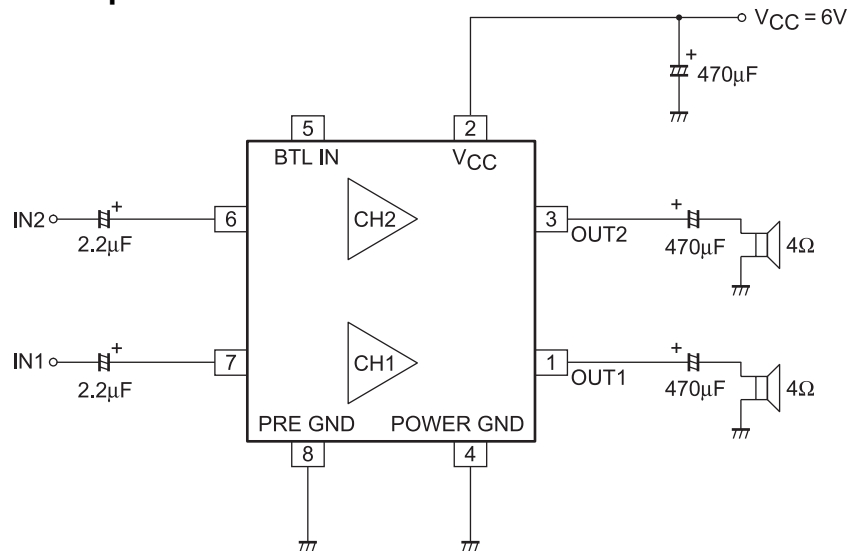


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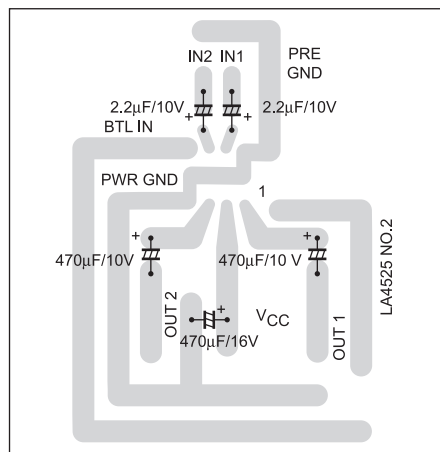
Block Diagram



Dual Operation Example



Sample Printed Circuit Pattern



Unit (capacitance : F)
65×65mm² (Cu-foiled area)

Pin Description

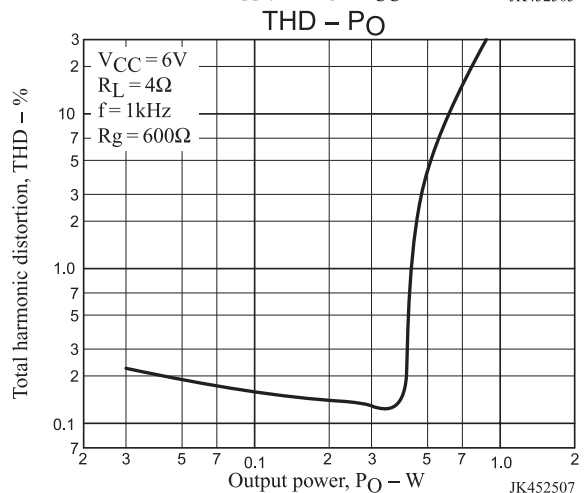
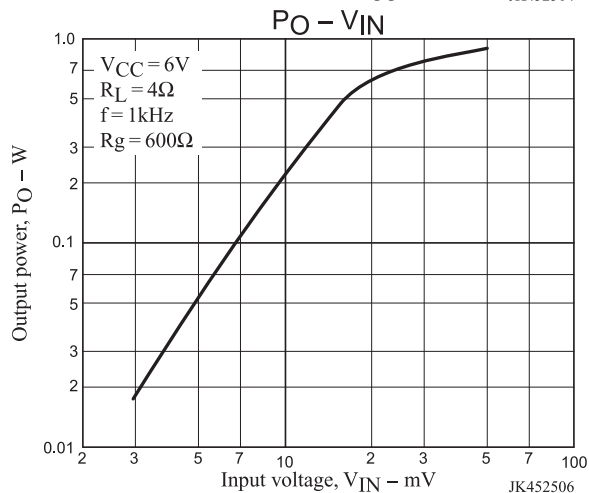
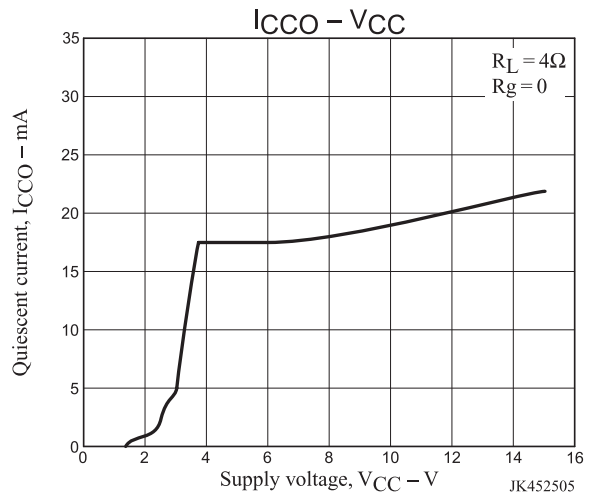
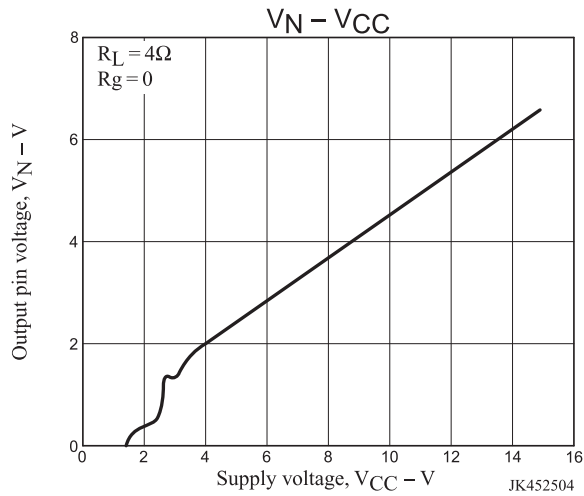
Number	Name	Description
1	OUT1	Channel 1 output
2	V _{CC}	Supply voltage
3	OUT2	Channel 2 output
4	POWER GND	Power amplifier ground
5	BTL IN	Bridge test load input
6	IN2	Channel 2 input
7	IN1	Channel 1 input
8	PRE GND	Preamplifier ground

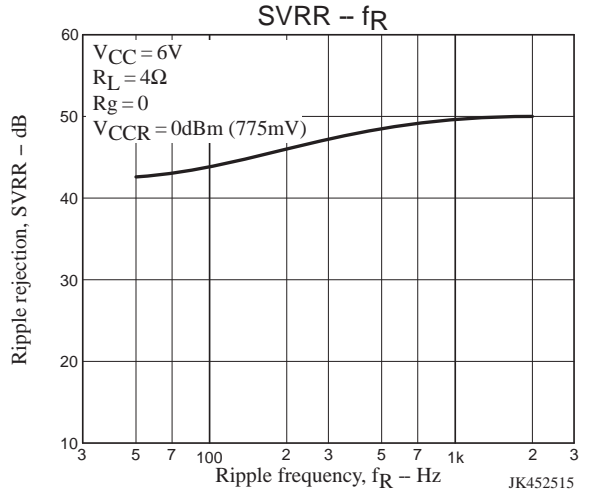
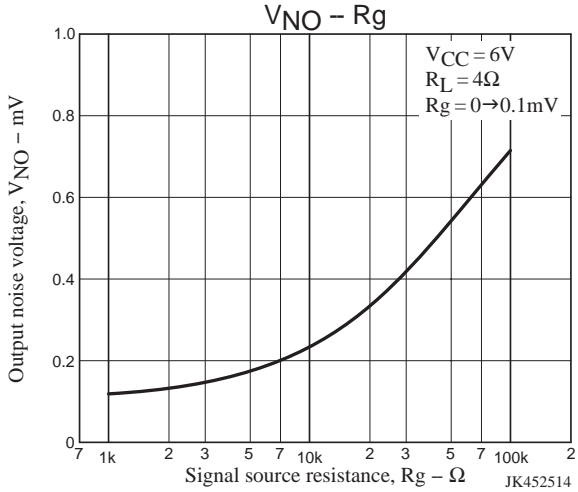
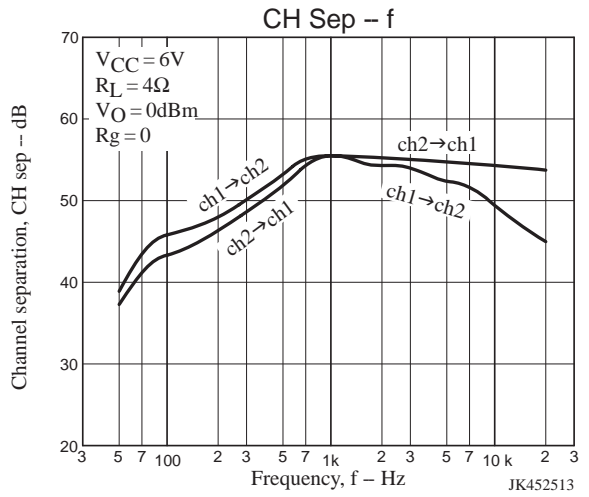
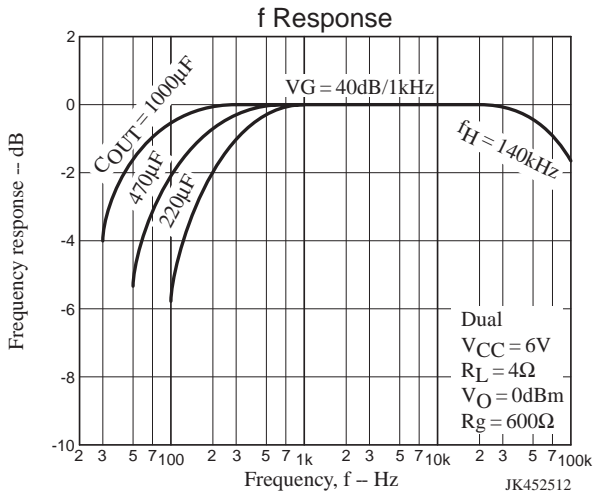
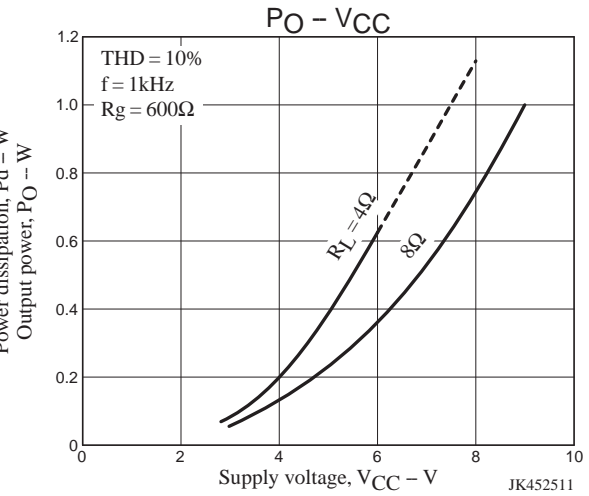
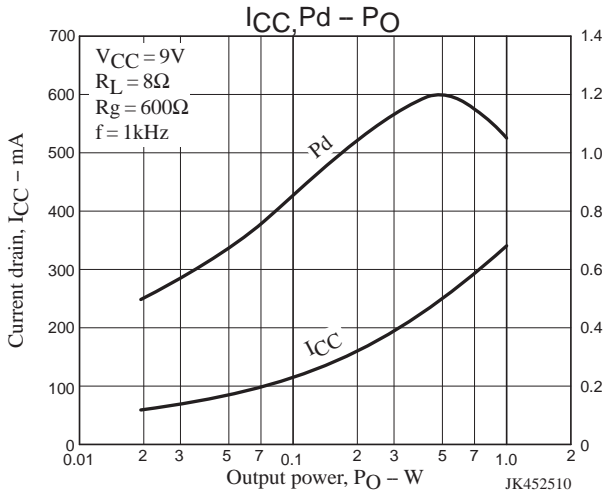
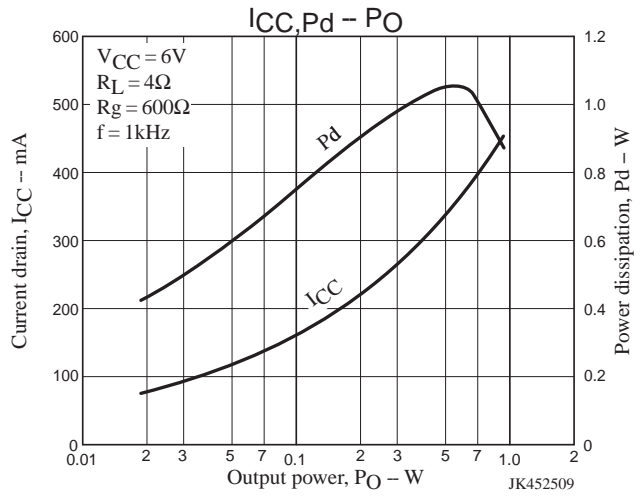
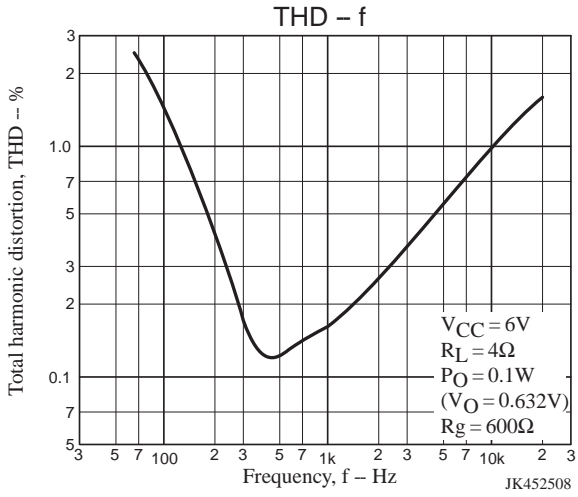
External Components Comparison

External components	Existing Sanyo ICs	LA4525
Output capacitors	○	○
Input capacitors	○	○
Bootstrap capacitors	○	×
Feedback capacitors	○	×
Filter capacitors	○	×
Oscillation damping mylars	○	×
Dual-mode operation total	11	4

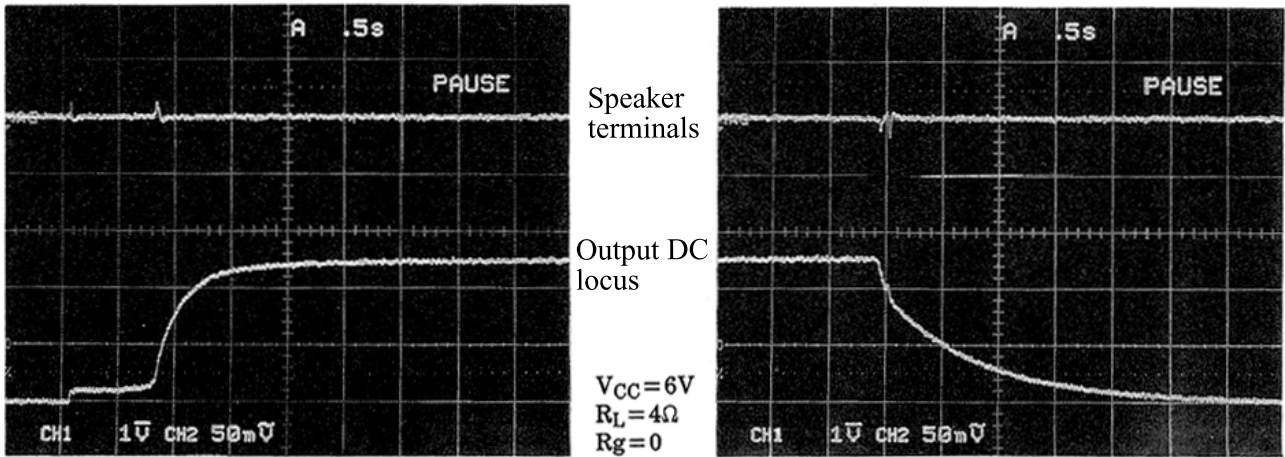
Pin Voltages

Pin number	Pin name	Pin voltage
1	OUT1	2.8V
2	V _{CC}	6V
3	OUT2	2.8V
4	POWER GND	0V
5	BTL IN	65mV
6	IN2	1.4V
7	IN1	1.4V
8	PRE GND	0V

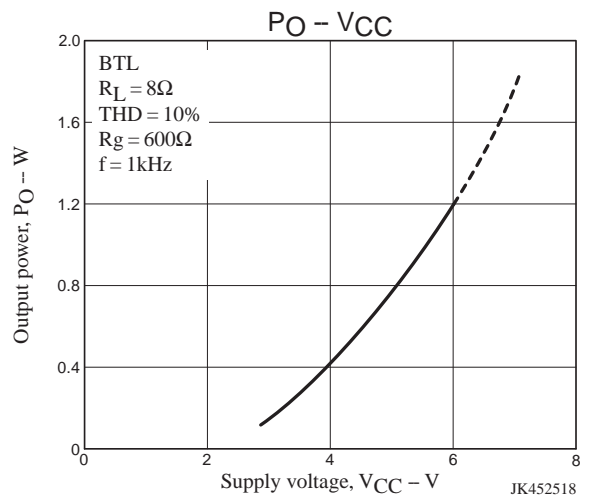
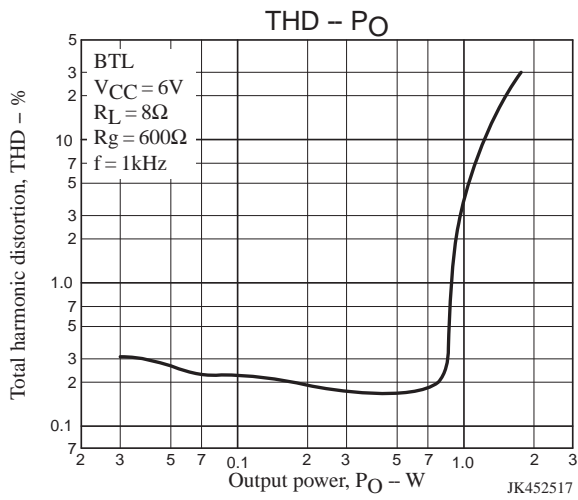
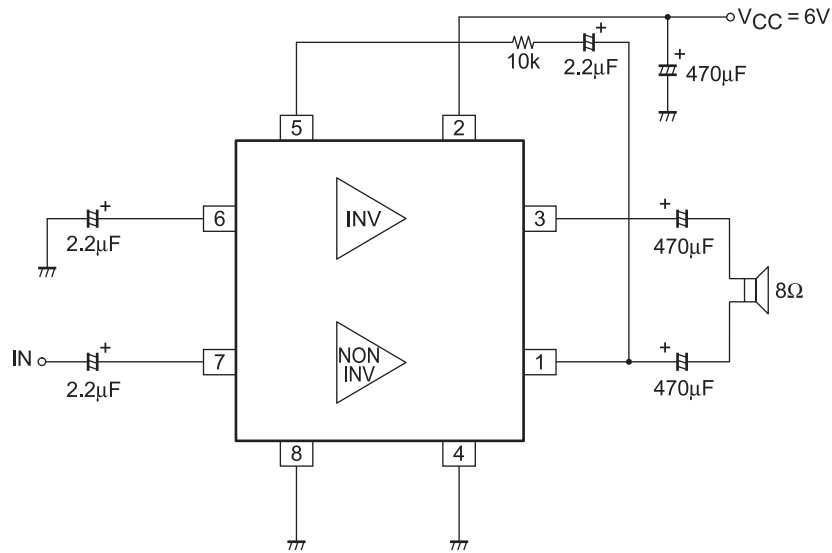


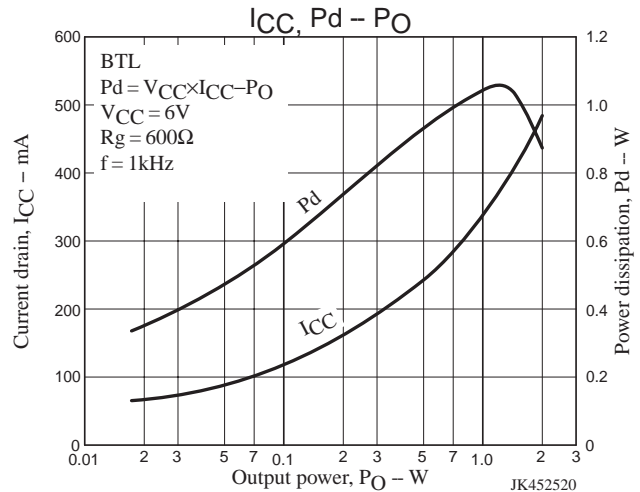
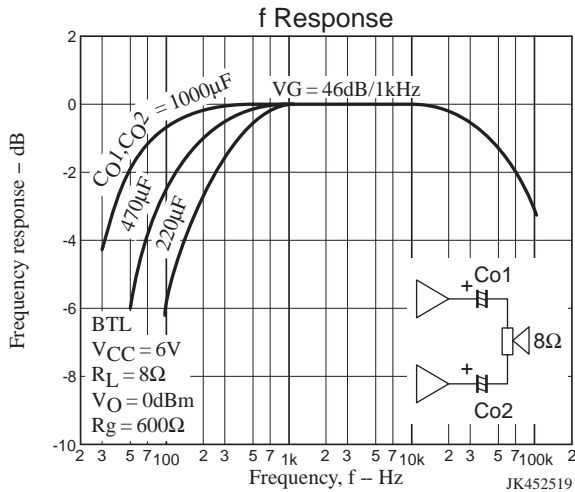


Rising and falling waveforms



BTL Operation Example





Handling Instructions and Precautions
Internal Circuits

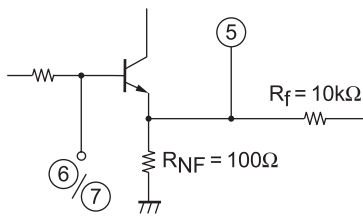


Figure 1. Input pins (6 and 7) and BTL input pin (5)

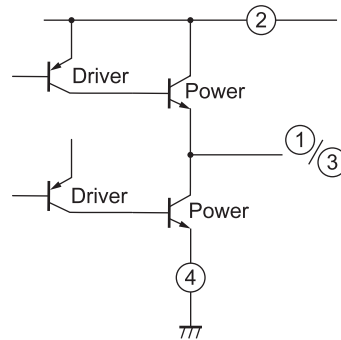
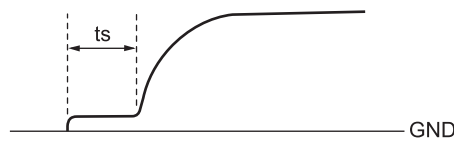


Figure 2. Output pins (1 and 3)

External Components

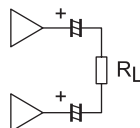
- The starting time, t_s , can be varied by changing the value of the input capacitor. A value of $2.2\mu\text{F}$ is recommended. A smaller value will result in a lower starting time, and a larger value, a higher starting time.



- The output capacitor should have a value of $470\mu\text{F}$. A lower value will cause the low-frequency roll-off and low-power characteristics to deteriorate.
- A value of $470\mu\text{F}$ is recommended for the power supply capacitor, although this can change according to the design setup conditions.
- In dual mode, BTL IN (the channel 2 negative feedback connection) should be left floating.

BTL mode

- The output capacitors should have a value of $470\mu\text{F}$. If these are omitted, a “popping” noise occurs. Also, any output offset will cause a current to flow which could damage the load under quiescent DC conditions.



- The output capacitors can be replaced with a single $220\mu\text{F}$ bipolar capacitor. A larger value can cause switching noise when power is applied to the device.

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- The voltage gain is fixed internally to 40dB in dual mode and 46dB in BTL mode. These values cannot be altered by connecting external components.
- Phase correction capacitance (600pF/TOTAL) is incorporated in the internal stages. Oscillation damping components (R and C) are also incorporated in the output pin circuits.
- Power consumption

Note that the 8-pin DIP does not have a heat dissipating surface and that the power dissipation ratings are critical. The maximum power dissipation of the device is 1.25W, and 1.5W when the device is mounted on the recommended PCB. The actual power dissipated depends on the supply voltage and the load conditions. Ensure that the device is kept within its maximum rating. For AC supplies, transformer tapings may need to be adjusted to keep the device within maximum ratings.

$$P_{d \max} = \frac{V_{CC}^2}{\pi^2 R_L} + I_{CCO} \times V_{CC}$$

Note

For BTL mode operation, the value of R_L used in the calculation should be 1/2 the actual value.

- If the speaker plug jacks short to ground when connected, a protection resistor should be inserted in the output line.
- If the device is operated at or near its rated values, these values can be exceeded by small changes in operating conditions, leading to device breakdown. Accordingly, ensure that a safety margin is maintained so as not to exceed the maximum ratings.
- Check the PCB surface after soldering to ensure that no pins have been accidentally shorted. Any short between pins could cause poor operating characteristics or permanently damage the device when power is applied.
- If making the PCB, check the printed wiring to ensure that no feedback loops occur between input and output.

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