STRUCTURE Silicon Monolithic Integrated Circuit
PRODUCT SERIES BTL Driver for car-CD
TYPE ＢＡ５８１４ＦＭ

PACKAGE OUTLINES	Figure 1 (Plastic Mold)	POWER DISSIPATION	Figure 2
BLOCK DIAGRAM	Figure 3	APPLICATION	Figure 4
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FUCTIONS
◎ 5ch Driver for BTL.
◎ Available in a HSOP-M28 power package
◎ Incorporates a thermal shut down circuit.
◎ Wide dynamic range（6.0V (Typ.) at Vcc=8V,RL=8Ω）
◎ Incorporates two trimmer regulator. （external PNP Tr.is necessary）

ABSOLUTE MAXIMUM RATINGS（Ta=25℃）

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	13.5	V
Power dissipation	Pd	2.2*	W
Operating temperature	Topr	-40～85	℃
Strage temperature	Tstg	-55～150	℃

Reduce power by 17.6mW for each degree above 25℃, on a glass epoxy PCB (70mm×70mm,1.6mm thick).

GUARANTEED OPERATING RANGES

Vcc	4.3 ～ 13.2 V

●Electrical characteristic （Unless otherwise noted, Ta=25℃, Vcc=8V,PVcc45=5V, BIAS=2.5V, RL=8Ω）

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions	Test circuit
Quiescent current	ICC	－	20	30	mA	input open	Figure 5
＜BTL Driver＞							
Output offset voltage	VOOF	-50	0	50	mV		Figure 5
High level output voltage 1	VOM1	5.4	6.0	－	V	CH1, 2, 3	Figure 5
High level output voltage 2	VOM2	3.6	4.0	－	V	CH4, 5	Figure 5
Closed loop voltage gain 1	GVC1	9.5	12.0	14.5	dB	CH1 RIN=10kΩ	Figure 5
Closed loop voltage gain 2	GVC2	15.5	18.0	20.5	dB	CH2 RIN=10kΩ	Figure 5
Closed loop voltage gain 3	GVC3	16.5	18.0	19.5	dB	CH3, 4, 5	Figure 5
Mute on voltage	VMTON	－	－	0.5	V		Figure 5
Mute off voltage	VMTOFF	2.0	－	－	V		Figure 5
Input current for mute pin	IMUTE	－	90	140	μA	VMUTE=5V	Figure 5
Input current for bias pin	IBIAS	－	75	120	μA		Figure 5
＜Regulator＞							
Threshold voltage of RE_I pin	VREITH	1.14	1.2	1.26	V		Figure 5
Output sink current of RE_O pin	ISIN	10	50	－	mA		Figure 5
Input bias current of RE_I pin	IBOP	－	20	300	nA		Figure 5

◎ This product is not designed for protection against radioactive rays.

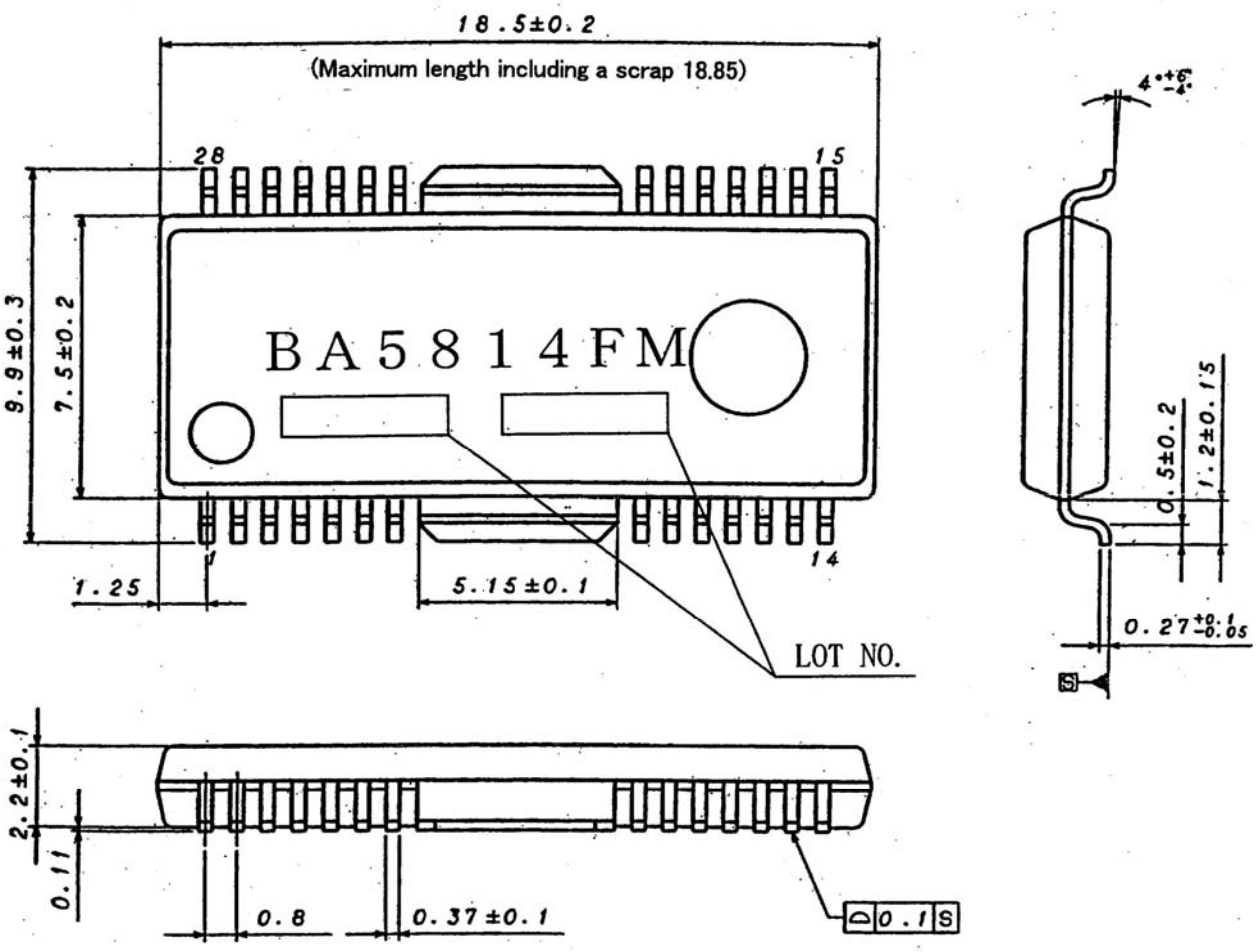
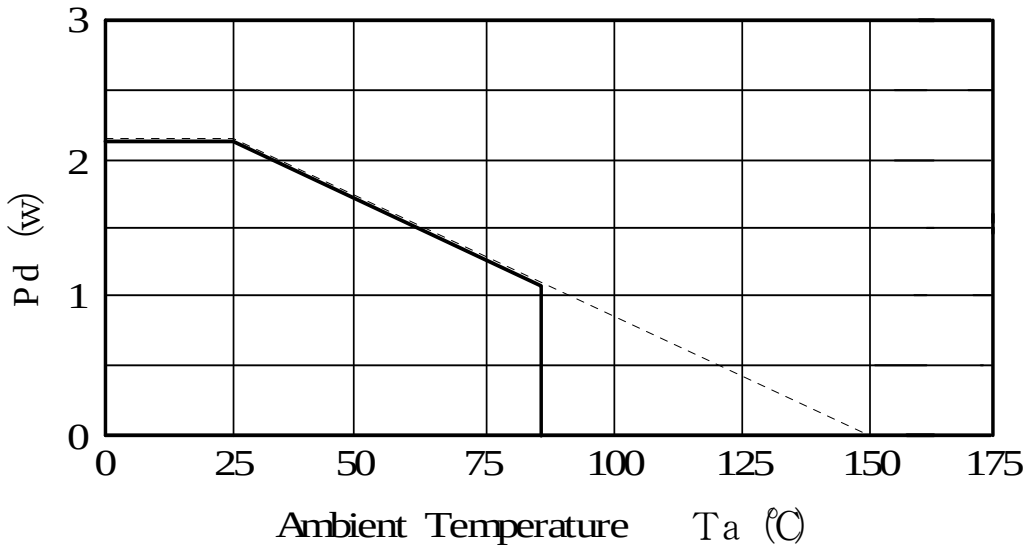


Figure 1

(UNIT: mm)

Figure No. : EX141-5001

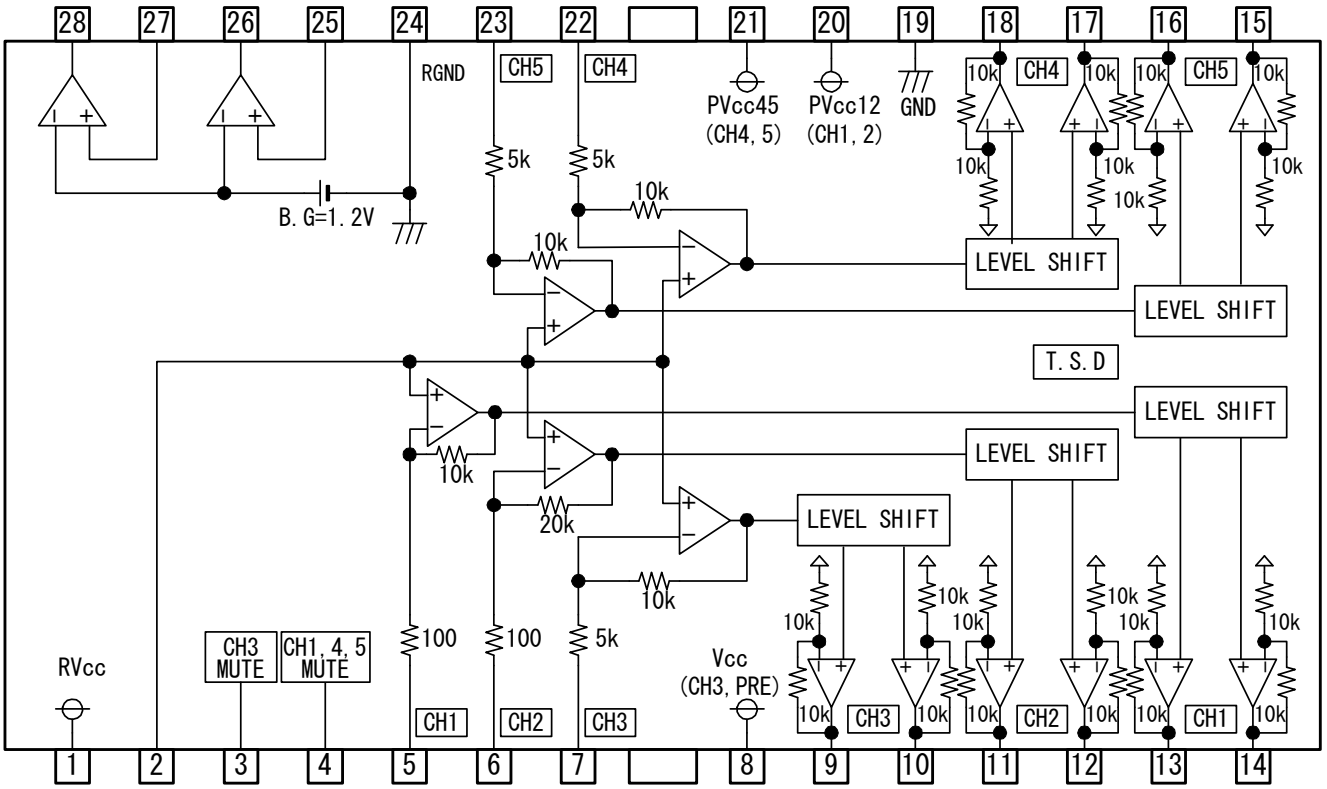
Power dissipation



Pd : power dissipation

Conditions : On less than 3% (percentage occupied by copper foil),
70mm×70mm 1.6mm thick, glass epoxy mounting.

Figure 2



Unit of resister［Ω］
T.S.D:Thermal shut down

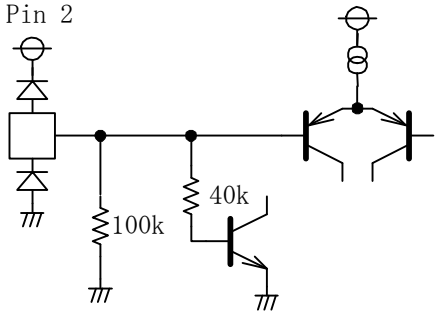
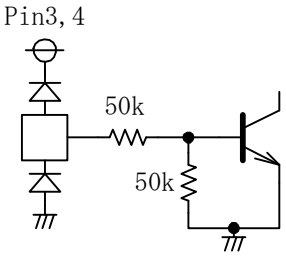
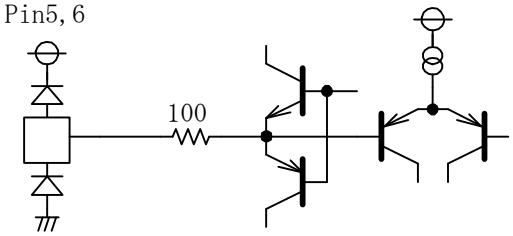
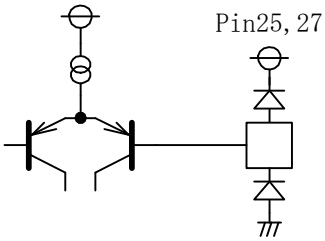
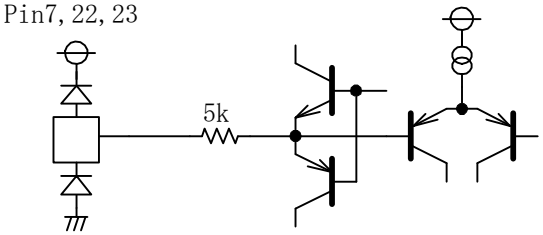
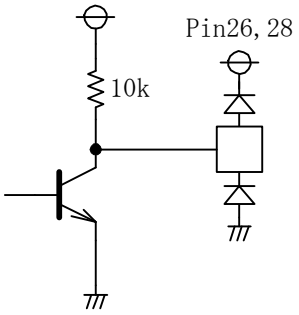
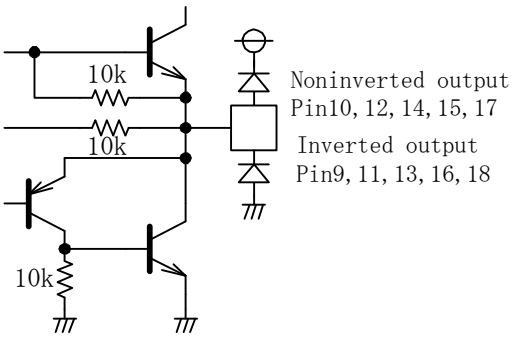
Figure 3

● 端子説明

No.	Symbol	Function	No.	Symbol	Function
1	RVcc	Vcc（for REG）	15	VO5(+)	Noninverted output of CH5
2	BIAS	Input for reference voltage (bias)	16	VO5(-)	Inverted output of CH5
3	MUTE1	CH3 Mute control	17	VO4(+)	Noninverted output of CH4
4	MUTE2	CH1,4,5 Mute control	18	VO4(-)	Inverted output of CH4
5	VIN1	Input for CH1	19	GND	GND（for PRE部、POWER）
6	VIN2	Input for CH2	20	PVcc12	Vcc（for CH1,2 POWER）
7	VIN3	Input for CH3	21	PVcc45	Vcc（for CH4,5 POWER）
8	VCC	Vcc（for PRE,CH3 POWER）	22	VIN4	Input for CH4
9	VO3(-)	Inverted output of CH3	23	VIN5	Input for CH5
10	VO3(+)	Noninverted output of CH3	24	RGND	GND（for REG）
11	VO2(-)	Inverted output of CH2	25	RE_I1	Regulator1 terminal of output feedback
12	VO2(+)	Noninverted output of CH2	26	RE_O1	Regulator1 terminal connected base of output transistor
13	VO1(-)	Inverted output of CH1	27	RE_I2	Regulator2 terminal of output feedback
14	VO1(+)	Noninverted output of CH1	28	RE_O2	Regulator2 terminal connected base of output transistor

notes) Symbol of + and – (output of drivers) means polarity to input pin.
(For example if voltage of pin.10 is high, pin,9 is low)

●Equivalent circuit of terminal

Bias	Mute1, 2
	
Input for driver(CH1, CH2)	**Regulator terminal of output feedback**
	
Input for driver(CH3, CH4, CH5)	**Regulator terminal connected base of external Tr**
	
Output of driver	
	

●Application circuit 1

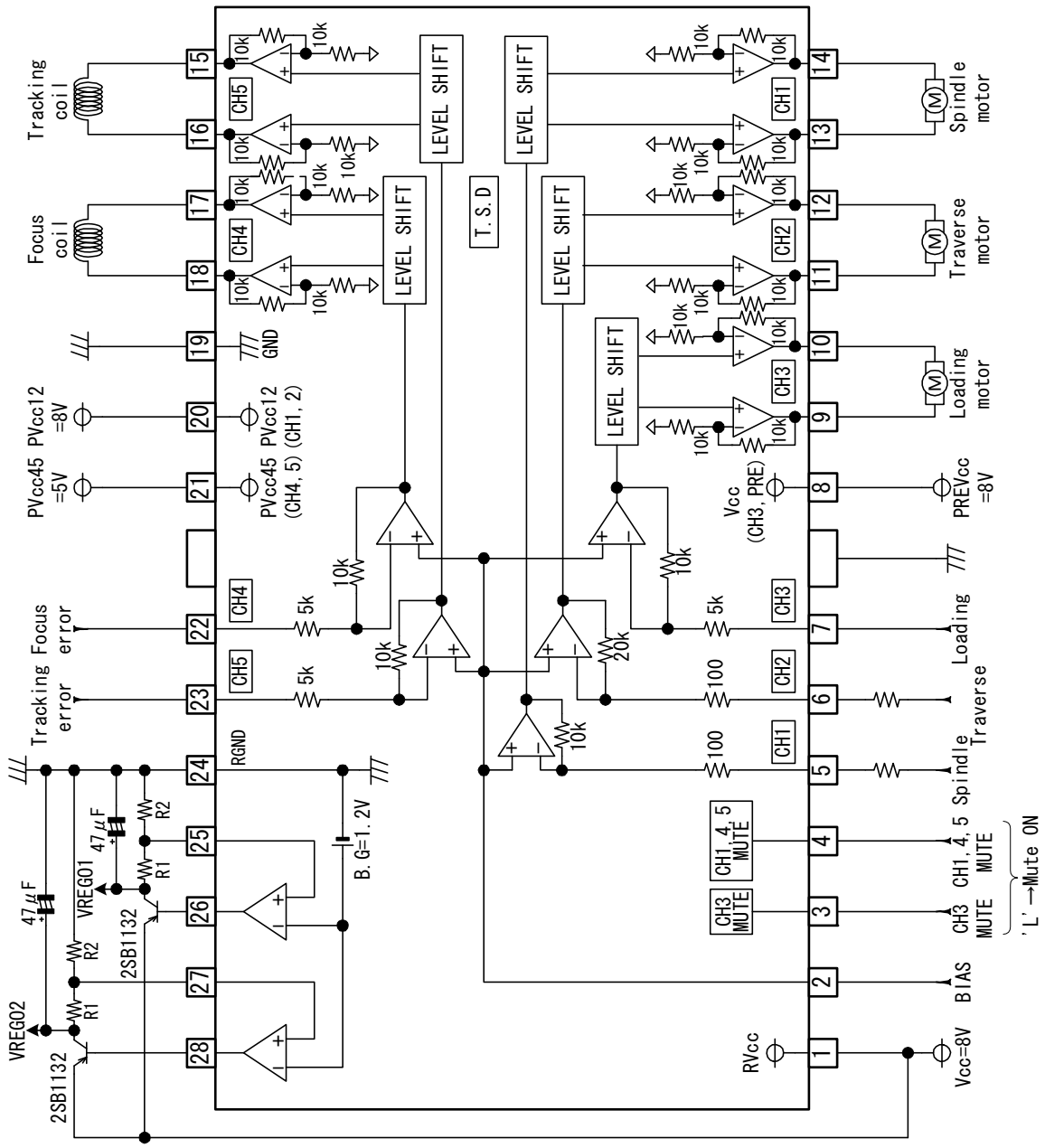


Figure 4

●Test circuit

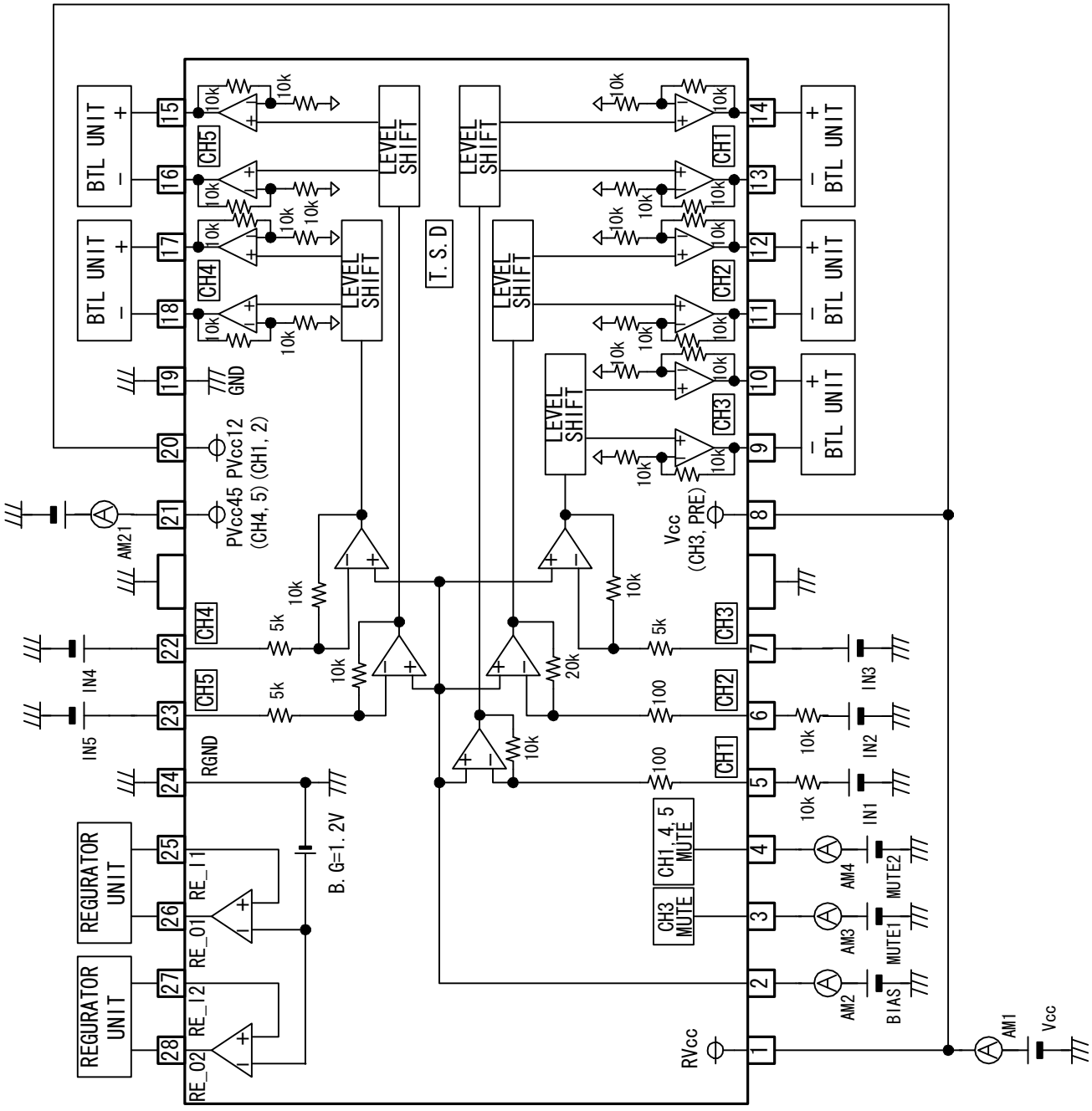
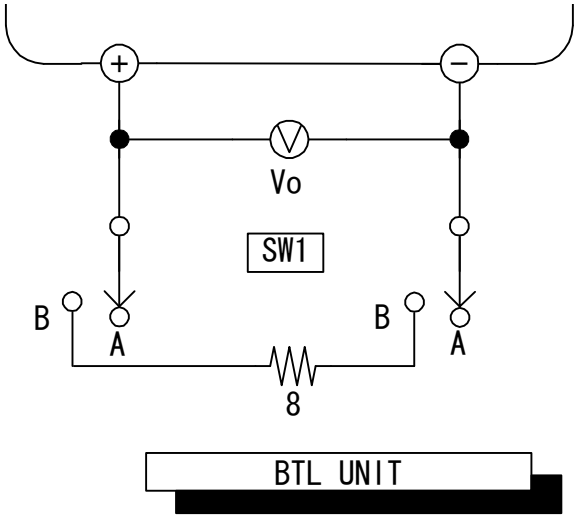


Figure 5

●Switch circuit



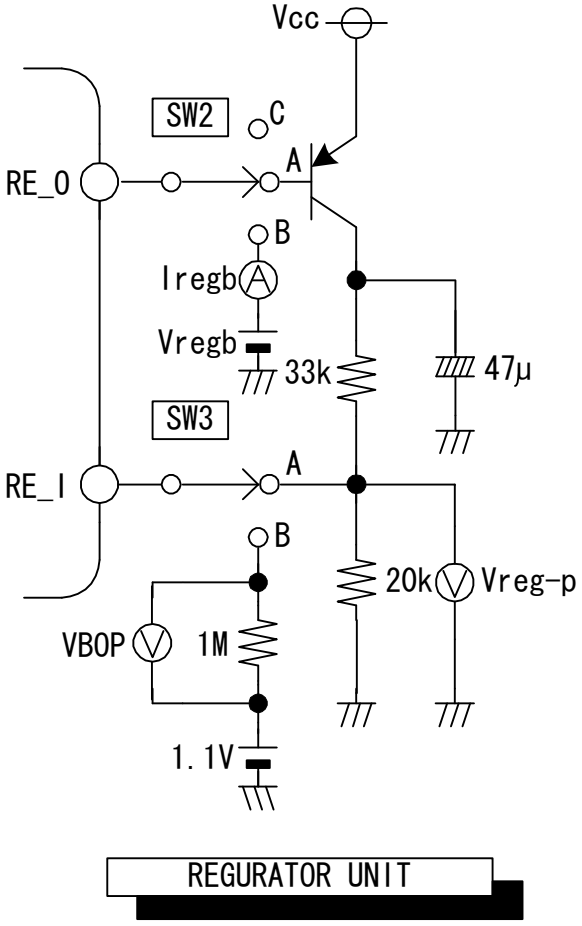


Figure 6

●Switch table

（※VCC=8V,PREVCC45=5V,BIAS=2.5V, SW=A position）

○Current of circuit　(MUTE=2V,BIAS=2.5V)

Parameter	Switch			Input voltage (V)			Comments	Test position
	1	2	3					
Quiescent current								AM1+AM21

○BTL Driver

Parameter	Switch			Input voltage (V)			Comments	Test position
	1	2	3	MUTE1,2	BIAS	VIN		
Output offset voltage	B			2.0	2.5	2.5		VO
High level output voltage	↓			↓	↓	5.0		VO
	↓			↓	↓	0		VO
Closed loop voltage gain	↓			↓	↓	2.8	20log{(VO-VOOF)/0.3}	VO
	↓			↓	↓	2.2	20log{(|VO|+VOOF)/0.3}	VO
Mute1,2 on voltage				0.5	↓	5.0	Output being mute	VO
Mute1,2 off voltage				2.0	↓	↓	Output being not mute	VO
Input current for mute pin				5.0	↓	2.5		AM3,AM4
Input current for bias pin				2.0	↓	↓		AM2

○Regulator

Parameter	Switch			Input voltage (V)			Comments	Test position
	1	2	3	MUTE	BIAS	Vregb		
Threshold voltage of RE_I pin				1.8	2.5	-		Vreg-p
Output sink current of RE_O pin		B		↓	↓	0.2		Iregb
Input bias current of RE_I pin		C	B	↓	↓	-	VBOP/(1M*2)	VBOP

●NOTES

1. Thermal shut down circuit built in.
When IC chip temperature rise to 175℃ (Typ.), output current is muted. And when IC chip temperature reach 150℃ (Typ.), the driver circuit starts up.

2. When mute-terminal (pin.3,4) voltage is open or lowered below 0.5V, output current is muted.
Under normal use condition, pull up the mute terminal above 1.5V
(3 pin → mute ch3 4 pin → mute ch1,4,5)

3. When bias-terminal (pin.2) voltage is below 0.7V (Typ.) ,driver is muted. Under normal use condition, set above 1.1V

4. When supply voltage falls below 3.7V (Typ.) , output current is muted. Next time supply voltage rises to 3.9V (Typ.) , the driver circuit start.

5. All drivers are muted by thermal shut down, supply voltage fall and bias voltage fall.
Output terminal of muted BTL driver applies internal bias voltage (PVCC/2(V)) .

6. Internal resistor allocate to input parts of driver have temperature characteristic about +1200ppm/℃ (Typ.).
Using external resister to change driver's gain, consider about temperature characteristic.

7. VREGO (output voltage of Regulator) is outputted with obtaining dispersion of VREITH (threshold voltage of RE_I pin) and external resistor. VREGO is described like under numerical formula by influence of IBOP, and choose the exact external resister on considering IBOP.

$$V_{REGO} = V_{REITH} \times \left(\frac{R_1}{R_2} + 1 \right) - R_1 \times I_{BOP} \quad (R_1, R_2 : \text{see page 7/11})$$

8. The capacitor between output of regulator and GND also has a property prevents oscillation.
Use capacitor with good temperature characteristic.

9. The supply voltage of regulator (pin 1) is partly one of internal current source. And GND of Regulator (pin 24) is partly one of internal current source.
When not using regulator, connect them to each external voltage supply and GND.

10. Insert the by-pass capacitor between Vcc-terminal and GND-terminal of IC as near as possible.
(approximately 0.1 μ F)

11. Heat dissipation fins are attached to the GND on the inside of the package.
Make sure to be connected to the external GND.

12. In principle, do not apply voltage below sub-potential of IC to terminal.
Examine in consideration of operation margin, when each driver output falls below sub-voltage of IC (GND) due to counter-electromotive-force of load.

13. Output pin is to avoid short-circuiting with PVcc and GND and other output pins. And, be fully careful in the direction of an integrated circuit on the substrate. An integrated circuit is damaged, and smoke may come out by the case.

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