

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)

DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM



UDG-92030-2

ABSOLUTE MAXIMUM RATINGS (Note 1)

| | |
|--|-----------------|
| Supply Voltage (Pins 13, 15) | 30V |
| Output Current, Source or Sink (Pins 11, 14) | |
| DC | 0.5A |
| Pulse (0.5 s) | 2.0A |
| Analog Inputs | |
| (Pins 1, 2, 7) | -0.3V to 7V |
| (Pin 8, 9) | -0.3V to 6V |
| Clock Output Current (Pin 4) | -5mA |
| Error Amplifier Output Current (Pin 3) | 5mA |
| Soft Start Sink Current (Pin 8) | 20mA |
| Oscillator Charging Current (Pin 5) | -5mA |
| Power Dissipation | 1W |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS



THERMAL RATINGS TABLE

| Package | Θ_{JA} | Θ_{JC} |
|---------|-----------------------|-------------------|
| DIL-16J | 80-120 | 28 ⁽²⁾ |
| DIL-16N | 90 ⁽¹⁾ | 45 |
| PLCC-20 | 43-75(1) | 34 |
| LCC-20 | 70-80 | 20 ⁽²⁾ |
| SOIC-16 | 50-120 ⁽¹⁾ | 35 |

(1) Specified Θ_{JA} (junction to ambient) is for devices mounted to 5in² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5in² aluminum PC board. Test PWB was 0.062in thick and typically used 0.635mm trace widths for power packages and 1.3mm trace widths for non-power packages with 100 x 100 mil probe land area at the end of each trace.

(2) Θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that the baseline values shown are worst case (mean +2s) for a 60 x 60mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack 10°C/W; pin grid array, 10°C/W.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for , $R_T = 3.65k$, $C_T = 1nF$, $V_{CC} = 15V$, $-55^{\circ}C < T_A < 125^{\circ}C$ for the UC1825, $-40^{\circ}C < T_A < 85^{\circ}C$ for the UC2825, and $0^{\circ}C < T_A < 70^{\circ}C$ for the UC3825, $T_A = T_O$.

| PARAMETERS | TEST CONDITIONS | UC1825 UC2825 | | | UC3825 | | | UNITS |
|-----------------------------------|-----------------------------------|------------------|------|------|--------|------|------|-----------------|
| | | MIN | TOP | MAX | MIN | TOP | MAX | |
| Reference Section | | | | | | | | |
| Output Voltage | $T_O = 25^{\circ}C$, $I_O = 1mA$ | 5.05 | 5.10 | 5.15 | 5.00 | 5.10 | 5.20 | V |
| Line Regulation | $10V < V_{CC} < 30V$ | | 2 | 20 | | 2 | 20 | mV |
| Load Regulation | $1mA < I_O < 10mA$ | | 5 | 20 | | 5 | 20 | mV |
| Temperature Stability* | $T_{MIN} < T_A < T_{MAX}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | mV/ $^{\circ}C$ |
| Total Output Variation* | Line, Load, Temperature | 5.00 | | 5.20 | 4.95 | | 5.25 | V |
| Output Noise Voltage* | $10Hz < f < 10kHz$ | | 50 | | | 50 | | μV |
| Long Term Stability* | $T_J = 125^{\circ}C$, 1000hrs. | | 5 | 25 | | 5 | 25 | mV |
| Short Circuit Current | $V_{REF} = 0V$ | -15 | -50 | -100 | -15 | -50 | -100 | mA |
| Oscillator Section | | | | | | | | |
| Initial Accuracy* | $T_J = 2^{\circ}C$ | 360 | 400 | 440 | 360 | 400 | 440 | kHz |
| Voltage Stability* | $10V < V_{CC} < 30V$ | | 0.2 | 2 | | 0.2 | 2 | % |
| Temperature Stability* | $T_{MIN} < T_A < T_{MAX}$ | | 5 | | | 5 | | % |
| Total Variation* | Line, Temperature | 340 | | 460 | 340 | | 460 | kHz |
| Oscillator Section (cont.) | | | | | | | | |
| Clock Out High | | 3.9 | 4.5 | | 3.9 | 4.5 | | V |
| Clock Out Low | | | 2.3 | 2.9 | | 2.3 | 2.9 | V |
| Ramp Peak* | | 2.6 | 2.8 | 3.0 | 2.6 | 2.8 | 3.0 | V |
| Ramp Valley* | | 0.7 | 1.0 | 1.25 | 0.7 | 1.0 | 1.25 | V |
| Ramp Valley to Peak* | | 1.6 | 1.8 | 2.0 | 1.6 | 1.8 | 2.0 | V |
| Error Amplifier Section | | | | | | | | |
| Input Offset Voltage | | | | 10 | | | 15 | mV |
| Input Bias Current | | | 0.6 | 3 | | 0.6 | 3 | μA |
| Input Offset Current | | | 0.1 | 1 | | 0.1 | 1 | μA |
| Open Loop Gain | $1V < V_O < 4V$ | 60 | 95 | | 60 | 95 | | dB |
| CMRR | $1.5V < V_{CM} < 5.5V$ | 75 | 95 | | 75 | 95 | | dB |
| PSRR | $10V < V_{CC} < 30V$ | 85 | 110 | | 85 | 110 | | dB |
| Output Sink Current | $V_{PIN3} = 1V$ | 1 | 2.5 | | 1 | 2.5 | | mA |
| Output Source Current | $V_{PIN3} = 4V$ | -0.5 | -1.3 | | -0.5 | -1.3 | | mA |
| Output High Voltage | $I_{PIN3} = -0.5mA$ | 4.0 | 4.7 | 5.0 | 4.0 | 4.7 | 5.0 | V |
| Output Low Voltage | $I_{PIN3} = 1mA$ | 0 | 0.5 | 1.0 | 0 | 0.5 | 1.0 | V |
| Unity Gain Bandwidth* | | 3 | 5.5 | | 3 | 5.5 | | MHz |
| Slew Rate* | | 6 | 12 | | 6 | 12 | | V/ μs |

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for , $R_T = 3.65k$, $C_T = 1nF$, $V_{CC} = 15V$, $-55^{\circ}C < T_A < 125^{\circ}C$ for the UC1825, $-40^{\circ}C < T_A < 85^{\circ}C$ for the UC2825, and $0^{\circ}C < T_A < 70^{\circ}C$ for the UC3825, $T_A = T_J$.

| PARAMETERS | TEST CONDITIONS | UC1825 UC2825 | | | UC3825 | | | UNITS |
|---|--|------------------|------|------|--------|------|------|---------|
| | | MIN | TOP | MAX | MIN | TOP | MAX | |
| PWM Comparator Section | | | | | | | | |
| Pin 7 Bias Current | $V_{PIN 7} = 0V$ | | -1 | -5 | | -1 | -5 | μA |
| Duty Cycle Range | | 0 | | 80 | 0 | | 85 | % |
| Pin 3 Zero DC Threshold | $V_{PIN 7} = 0V$ | 1.1 | 1.25 | | 1.1 | 1.25 | | V |
| Delay to Output* | | | 50 | 80 | | 50 | 80 | ns |
| Soft-Start Section | | | | | | | | |
| Charge Current | $V_{PIN 8} = 0.5V$ | 3 | 9 | 20 | 3 | 9 | 20 | μA |
| Discharge Current | $V_{PIN 8} = 1V$ | 1 | | | 1 | | | mA |
| Current Limit / Shutdown Section | | | | | | | | |
| Pin 9 Bias Current | $0 < V_{PIN 9} < 4V$ | | | 15 | | | 10 | μA |
| Current Limit Threshold | | 0.9 | 1.0 | 1.1 | 0.9 | 1.0 | 1.1 | V |
| Shutdown Threshold | | 1.25 | 1.40 | 1.55 | 1.25 | 1.40 | 1.55 | V |
| Delay to Output | | | 50 | 80 | | 50 | 80 | ns |
| Output Section | | | | | | | | |
| Output Low Level | $I_{OUT} = 20mA$ | | 0.25 | 0.40 | | 0.25 | 0.40 | V |
| | $I_{OUT} = 200mA$ | | 1.2 | 2.2 | | 1.2 | 2.2 | V |
| Output High Level | $I_{OUT} = -20mA$ | 13.0 | 13.5 | | 13.0 | 13.5 | | V |
| | $I_{OUT} = -200mA$ | 12.0 | 13.0 | | 12.0 | 13.0 | | V |
| Collector Leakage | $V_C = 30V$ | | 100 | 500 | | 10 | 500 | μA |
| Rise/Fall Time* | $CL = 1nF$ | | 30 | 60 | | 30 | 60 | ns |
| Under-Voltage Lockout Section | | | | | | | | |
| Start Threshold | | 8.8 | 9.2 | 9.6 | 8.8 | 9.2 | 9.6 | V |
| UVLO Hysteresis | | 0.4 | 0.8 | 1.2 | 0.4 | 0.8 | 1.2 | V |
| Supply Current Section | | | | | | | | |
| Start Up Current | $V_{CC} = 8V$ | | 1.1 | 2.5 | | 1.1 | 2.5 | mA |
| ICC | $V_{PIN 1}, V_{PIN 7}, V_{PIN 9} = 0V; V_{PIN 2} = 1V$ | | 22 | 33 | | 22 | 33 | mA |

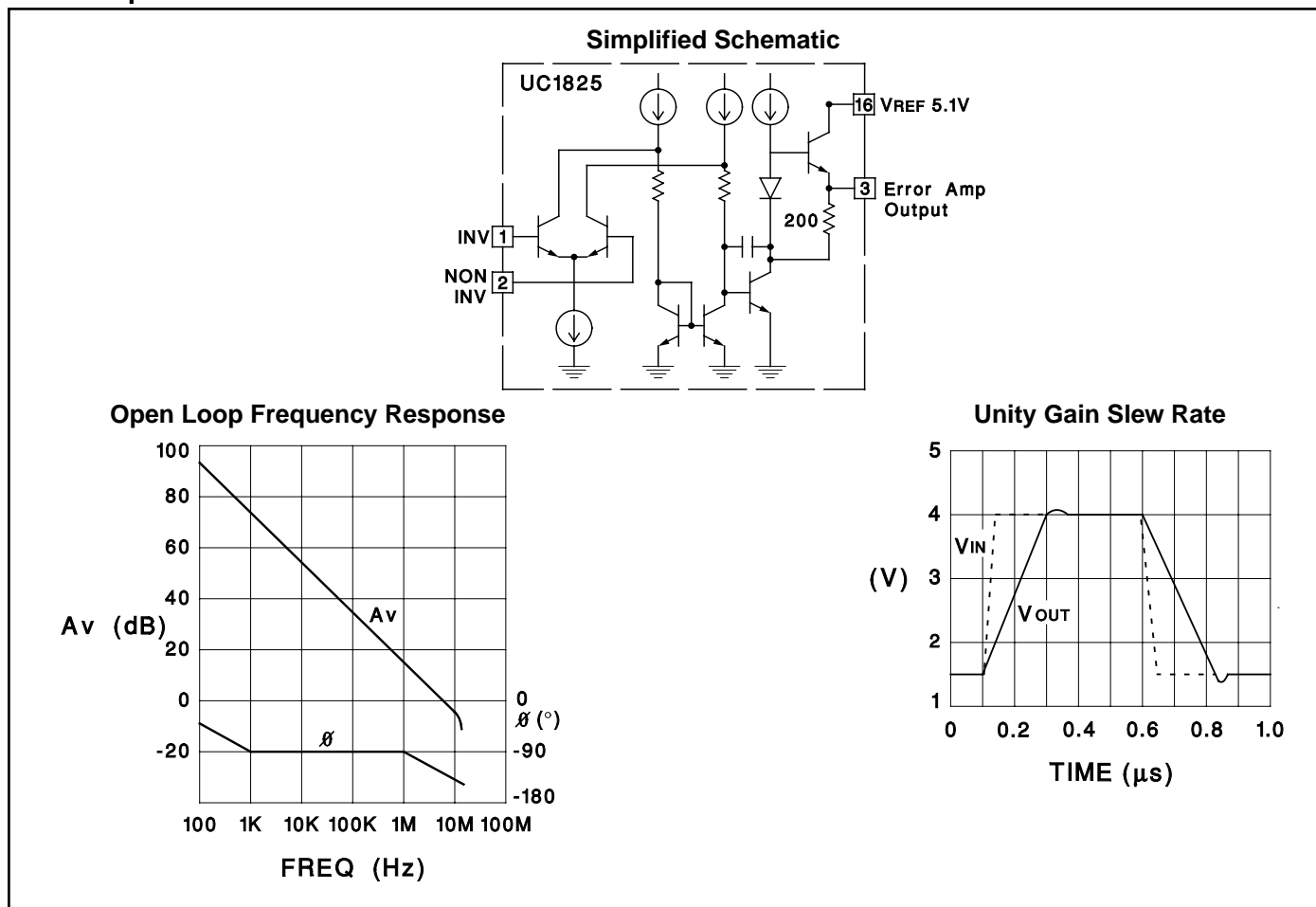
* This parameter not 100% tested in production but guaranteed by design.

Printed Circuit Board Layout Considerations

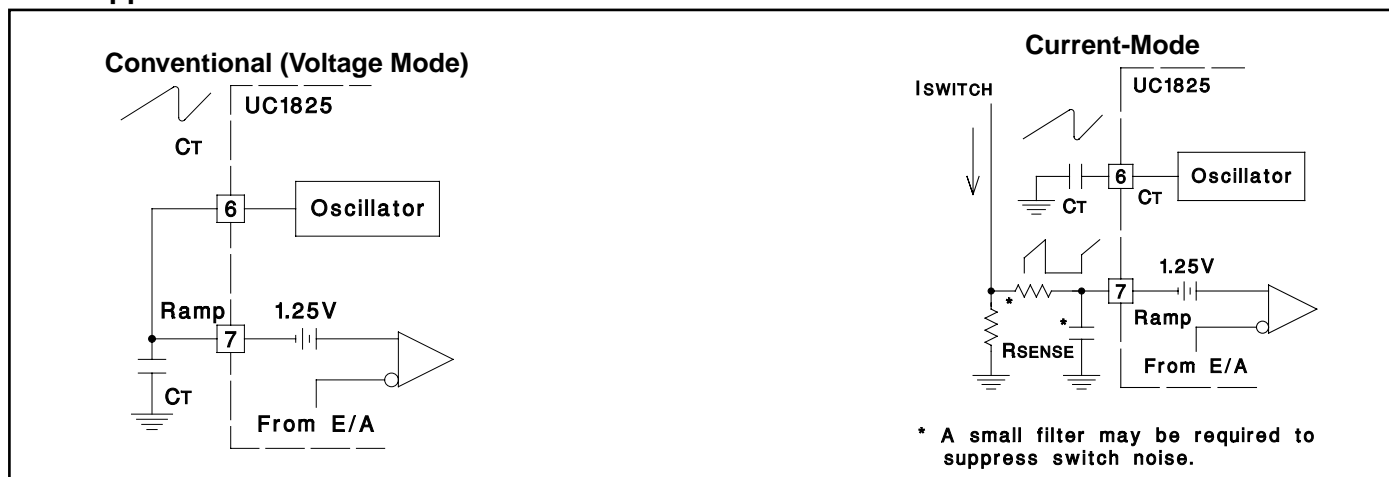
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve

this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1 μ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

Error Amplifier Circuit



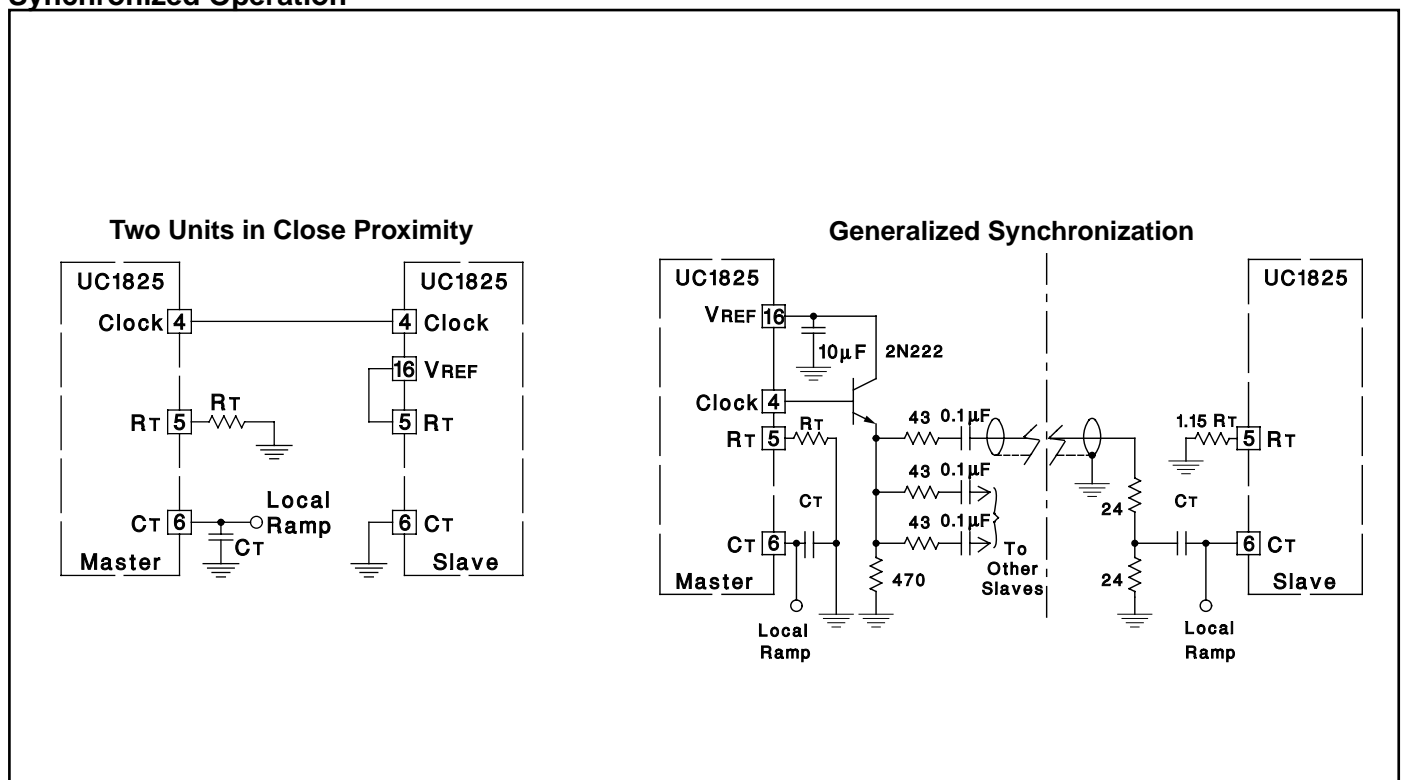
PWM Applications



Oscillator Circuit



Synchronized Operation

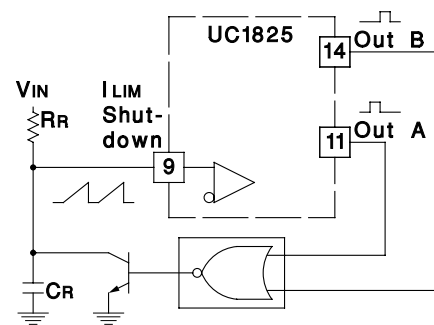


Forward Technique for Off-Line Voltage Mode Application



Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



Output Section

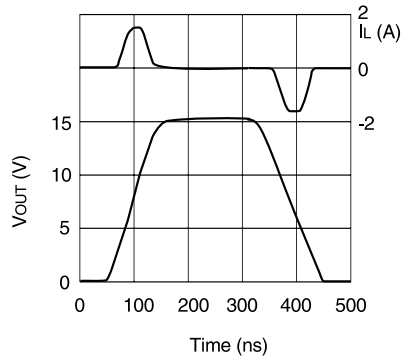
Simplified Schematic



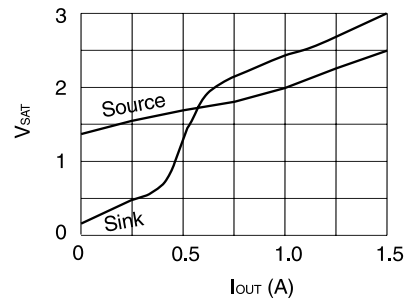
Rise/Fall Time ($C_L=1nF$)



Rise/Fall Time ($C_L=10nF$)



Saturation Curves



Open Loop Laboratory Test Fixture



Design Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-87681012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-87681012A UC1825L/ 883B | Samples |
| 5962-8768101EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8768101EA UC1825J/883B | Samples |
| 5962-8768101QFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8768101QF A UC1825W/883B | Samples |
| UC1825J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | UC1825J | Samples |
| UC1825J883B | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8768101EA UC1825J/883B | Samples |
| UC1825L | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | UC1825L | Samples |
| UC1825L883B | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-87681012A UC1825L/ 883B | Samples |
| UC1825W883B | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-8768101QF A UC1825W/883B | Samples |
| UC2825DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2825DW | Samples |
| UC2825DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2825DW | Samples |
| UC2825DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2825DW | Samples |
| UC2825DWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2825DW | Samples |
| UC2825J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -40 to 85 | UC2825J | Samples |
| UC2825N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | UC2825N | Samples |
| UC2825NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | UC2825N | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| UC2825Q | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | UC2825Q | Samples |
| UC2825QG3 | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | UC2825Q | Samples |
| UC2825QTR | OBSOLETE | PLCC | FN | 20 | | TBD | Call TI | Call TI | -40 to 85 | UC2825Q | |
| UC2825QTRG3 | ACTIVE | PLCC | FN | 20 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| UC3825DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3825DW | Samples |
| UC3825DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3825DW | Samples |
| UC3825DWTR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3825DW | Samples |
| UC3825DWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3825DW | Samples |
| UC3825J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | 0 to 70 | UC3825J | Samples |
| UC3825N | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3825N | Samples |
| UC3825NG4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3825N | Samples |
| UC3825Q | ACTIVE | PLCC | FN | 20 | 46 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | 0 to 70 | UC3825Q | Samples |
| UC3825QTR | ACTIVE | PLCC | FN | 20 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | 0 to 70 | UC3825Q | Samples |
| UC3825QTRG3 | ACTIVE | PLCC | FN | 20 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | 0 to 70 | UC3825Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1825, UC2825, UC2825M, UC3825, UC3825M :

● Catalog: [UC3825](#), [UC2825](#), [UC3825M](#), [UC3825](#)

● Military: [UC2825M](#), [UC1825](#)

● Space: [UC1825-SP](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

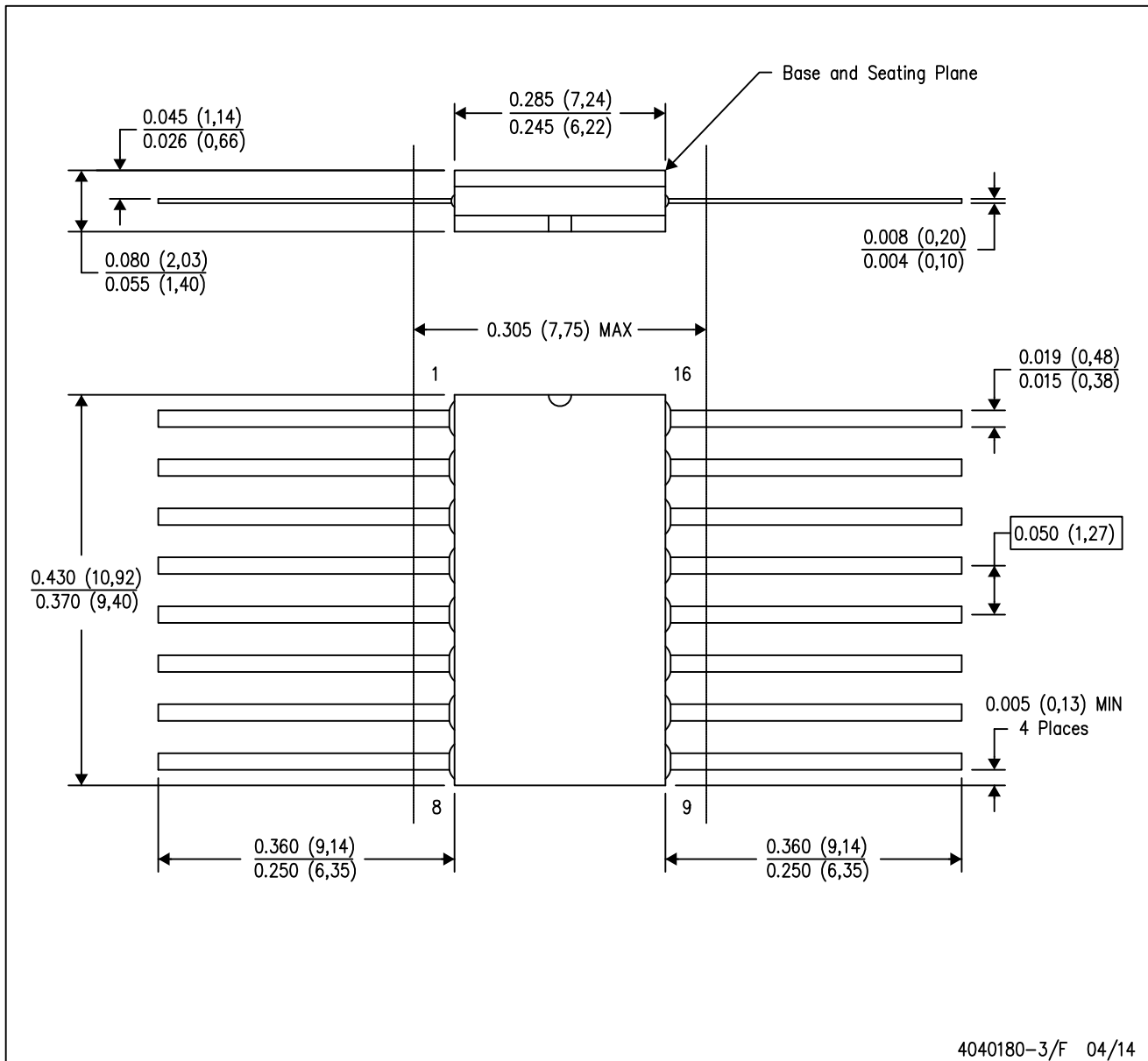


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

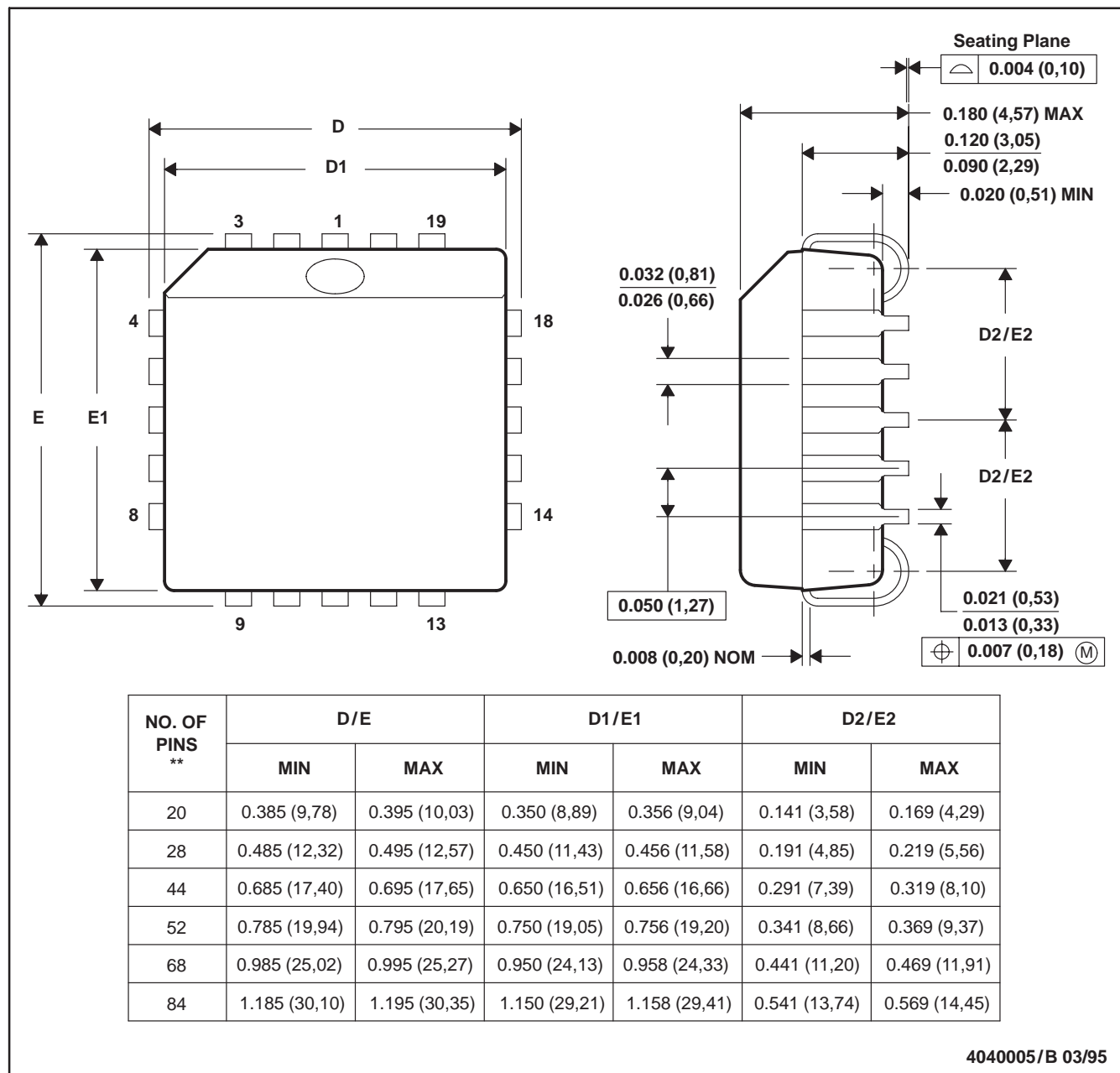


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

DW (R-PDSO-G16)

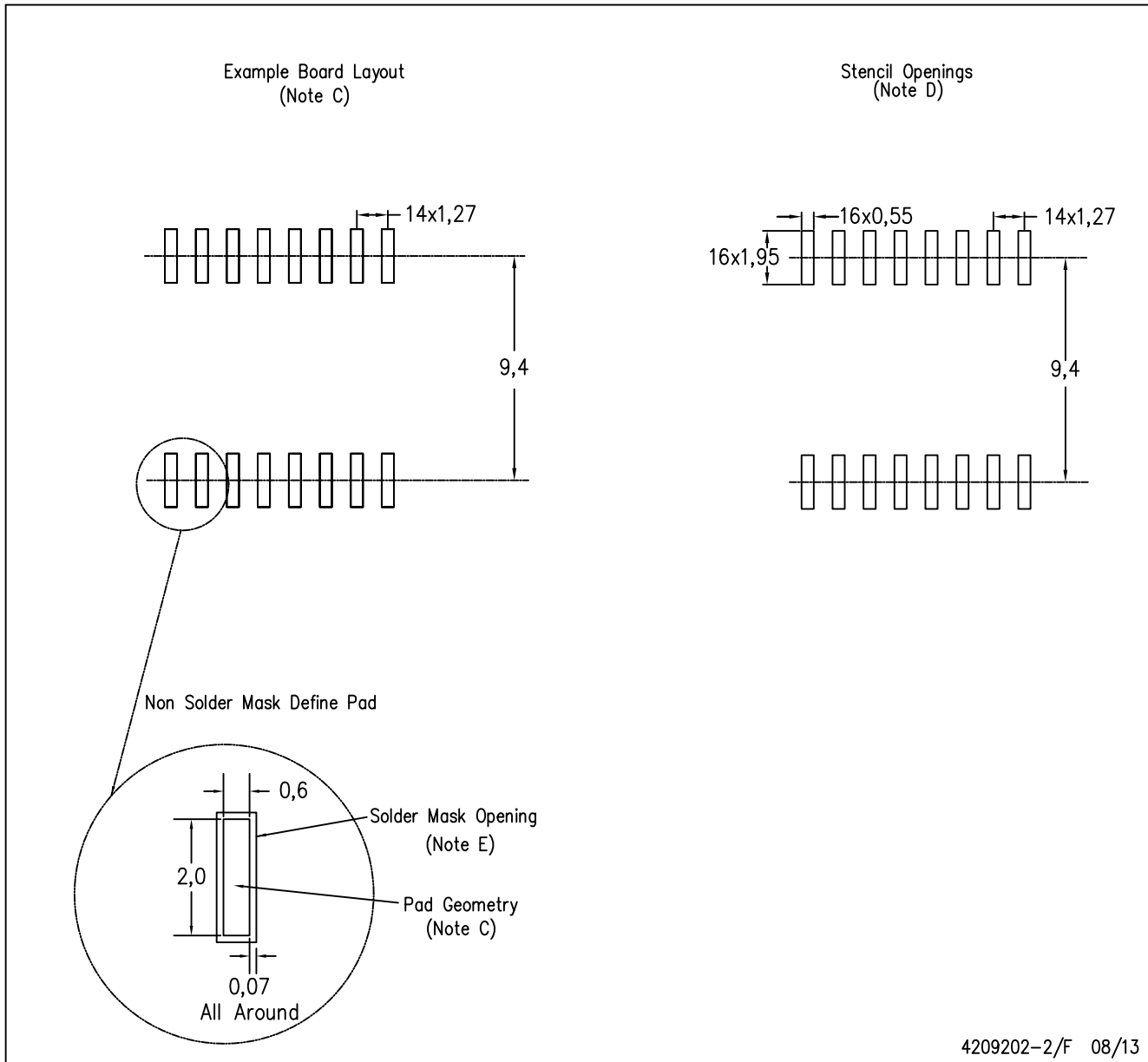
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4209202-2/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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