

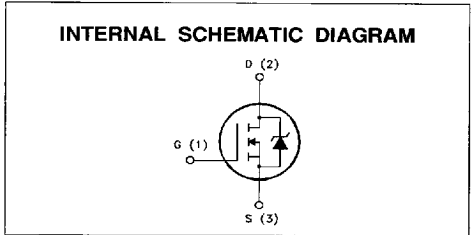
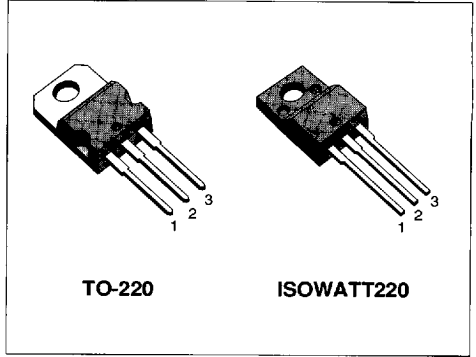
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR**

TYPE	V _{DSS}	R _{DS(on)}	I _D
STP40N10	100 V	< 0.04 Ω	40 A
STP40N10FI	100 V	< 0.04 Ω	22 A

- TYPICAL R_{DS(on)} = 0.035 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP40N10	STP40N10FI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100		V
V _{GS}	Gate-source Voltage	± 20		V
I _D	Drain Current (continuous) at T _c = 25 °C	40	22	A
I _D	Drain Current (continuous) at T _c = 100 °C	28	15	A
I _{DM} (*)	Drain Current (pulsed)	160	160	A
P _{tot}	Total Dissipation at T _c = 25 °C	150	45	W
	Derating Factor	1	0.3	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	—	2000	V
T _{stg}	Storage Temperature	-65 to 175		°C
T _j	Max. Operating Junction Temperature	175		°C

(*) Pulse width limited by safe operating area

THERMAL DATA

			TO-220	ISOWATT220	
$R_{thj-case}$	Thermal Resistance Junction-case	Max	1	3.33	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max		62.5	°C/W
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ		0.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose			300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	40	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	210	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	50	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100\text{ }^\circ\text{C}$, pulse width limited by T_j max, $\delta < 1\%$)	28	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ }^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125\text{ }^\circ\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2	2.9	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 20\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 20\text{ A}$ $T_c = 100\text{ }^\circ\text{C}$		0.035	0.04 0.08	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	40			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 20\text{ A}$	14	25		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		2150	2800	pF
C_{oss}	Output Capacitance			600	800	pF
C_{rss}	Reverse Transfer Capacitance			150	200	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		20 130	30 190	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 80\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		500		A/ μ s
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80\text{ V}$ $I_D = 40\text{ A}$ $V_{GS} = 10\text{ V}$		70 12 30	100	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(off)}$ t_f	Off-voltage Rise Time Fall Time	$V_{DD} = 80\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$		50 70	70 100	ns ns
t_c	Cross-over Time	(see test circuit, figure 5)		140	200	ns

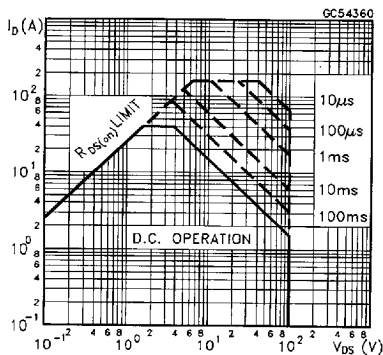
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\ast)$	Source-drain Current Source-drain Current (pulsed)				40 160	A A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 40\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 40\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		130		ns
Q_{rr}	Reverse Recovery Charge			0.65		μ C
I_{RRM}	Reverse Recovery Current			10		A

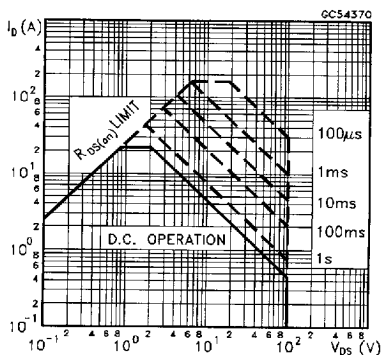
(*) Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

(*) Pulse width limited by safe operating area

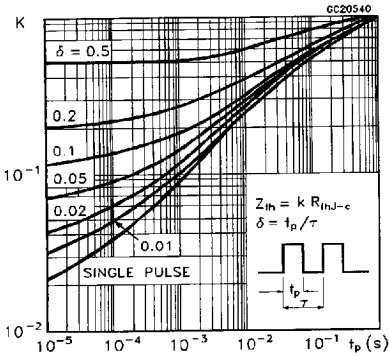
Safe Operating Areas For TO-220



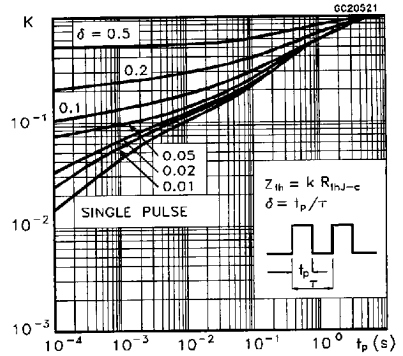
Safe Operating Areas For ISOWATT220



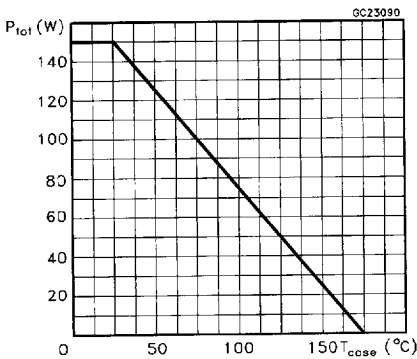
Thermal Impedance For TO-220



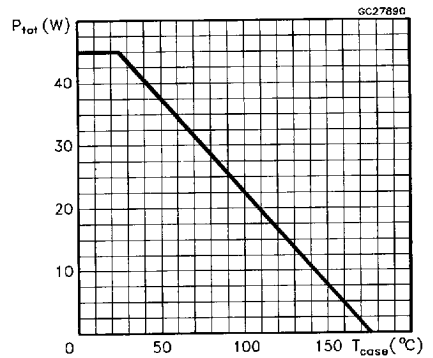
Thermal Impedance For ISOWATT220



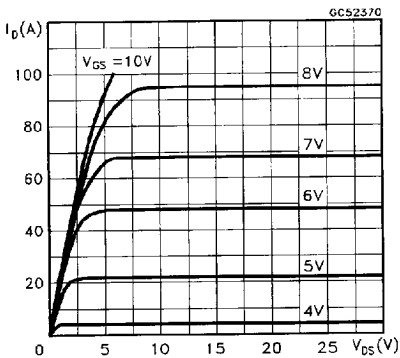
Derating Curve For TO-220



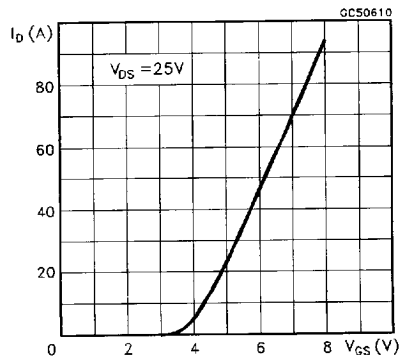
Derating Curve For ISOWATT220



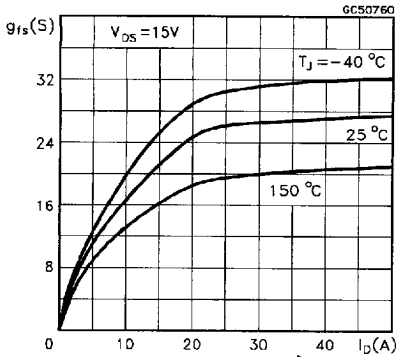
Output Characteristics



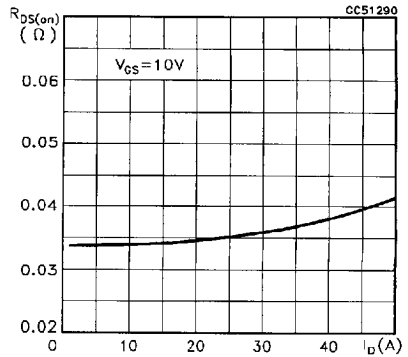
Transfer Characteristics



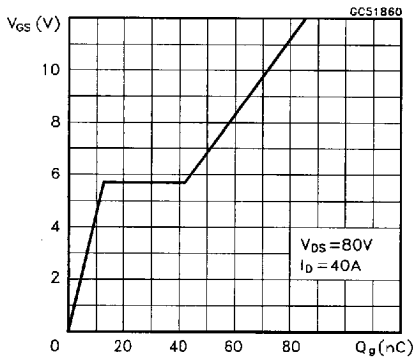
Transconductance



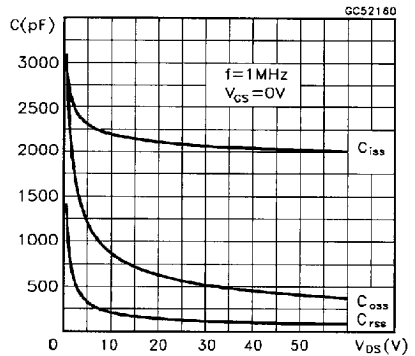
Static Drain-source On Resistance



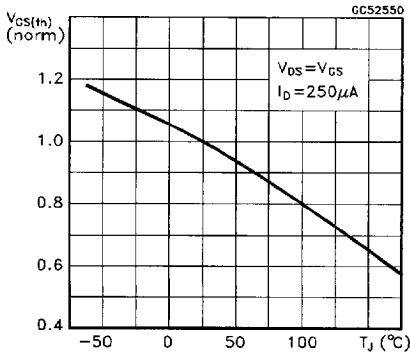
Gate Charge vs Gate-source Voltage



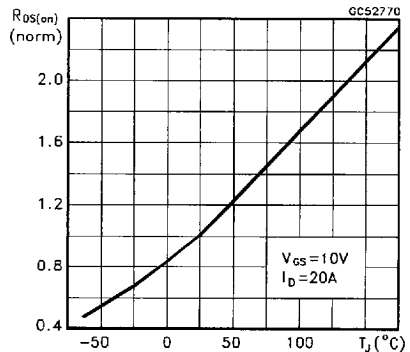
Capacitance Variations



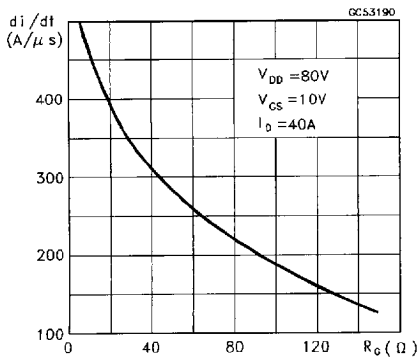
Normalized Gate Threshold Voltage vs Temperature



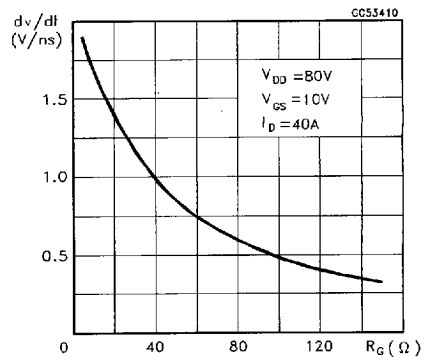
Normalized On Resistance vs Temperature



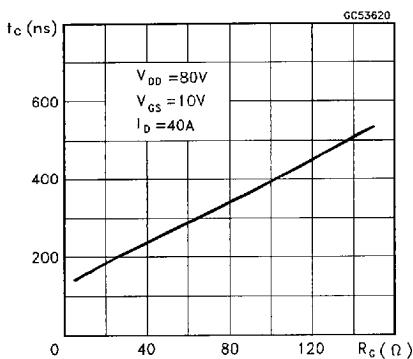
Turn-on Current Slope



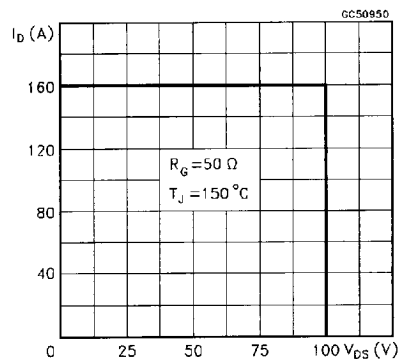
Turn-off Drain-source Voltage Slope



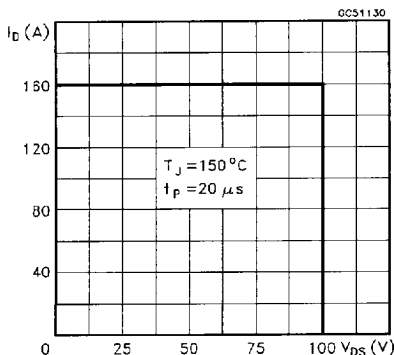
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

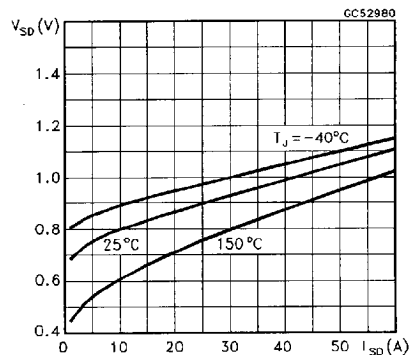


Fig. 1: Unclamped Inductive Load Test Circuits

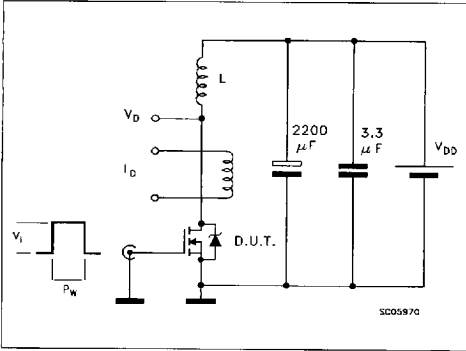


Fig. 2: Unclamped Inductive Waveforms

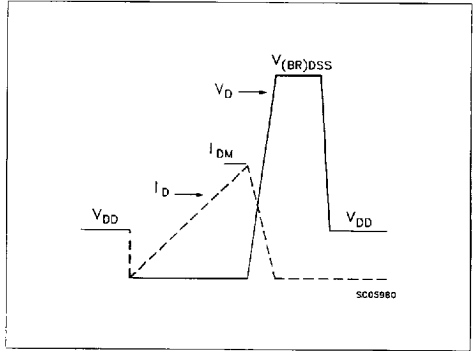


Fig. 3: Switching Times Test Circuits For Resistive Load

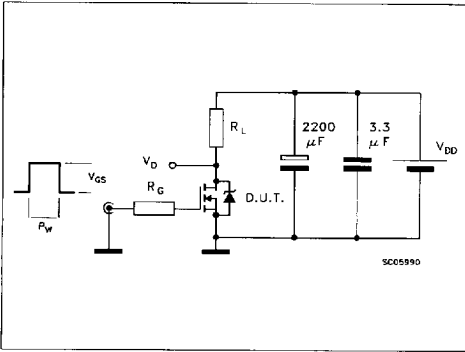


Fig. 4: Gate Charge Test Circuit

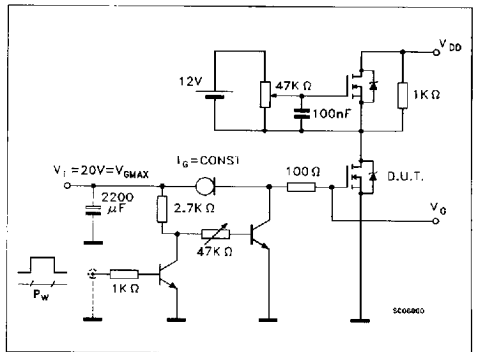


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time

